SDE-1000/3000 SERVICE NOTES

First Edition

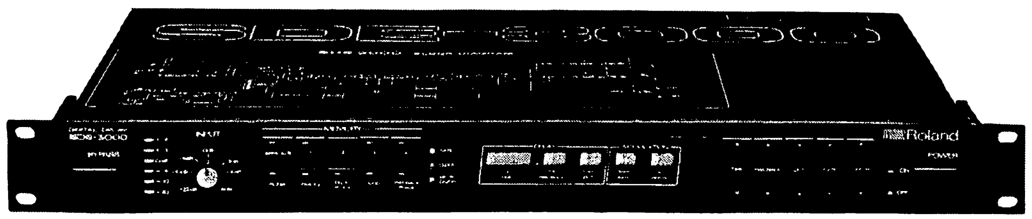


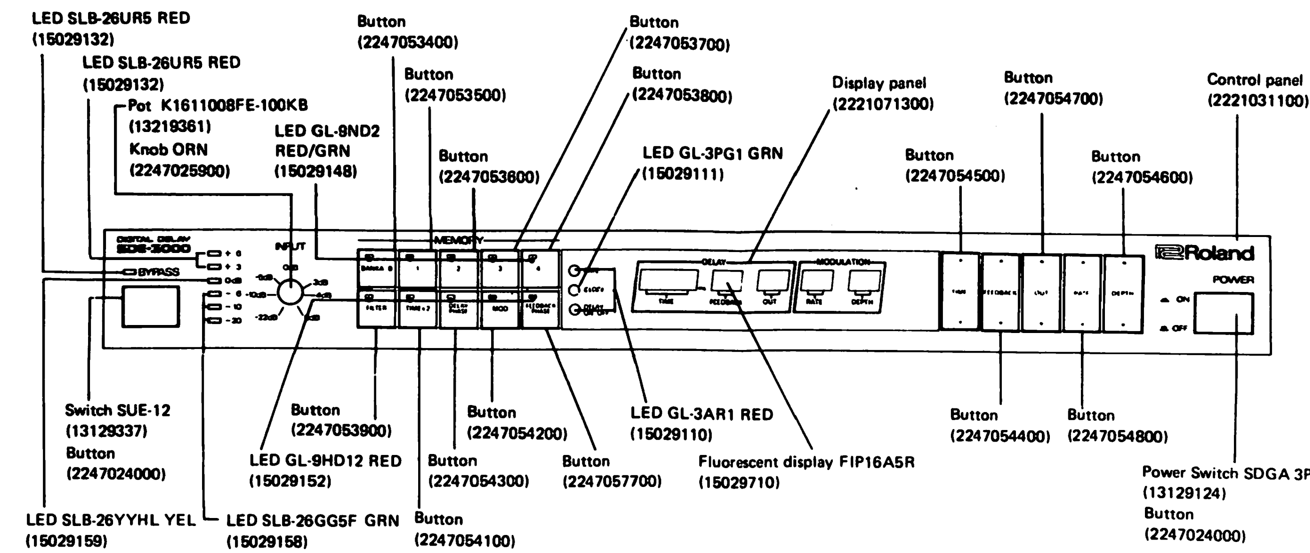
PHOTO SDE-3000

SPECIFICATIONS

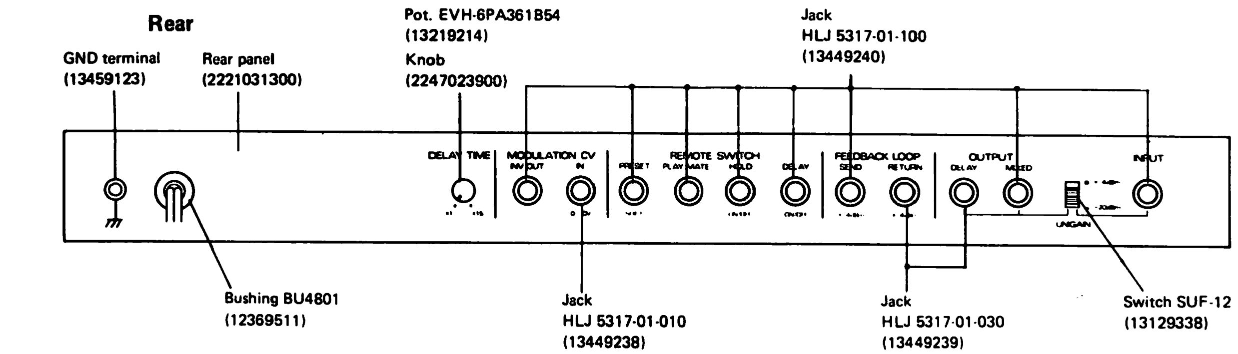
		SDE-1000	SDE-3000
Input	Level Impedance	−20dBm (−3dBm max.) −35dBm (−18dBm max.) 560kΩ (−20dBm) 560kΩ (−35dBm)	+4dBm (+16dBm max.) −20dBm (−8dBm max.) 56kΩ (+4dBm) 560kΩ (−20dBm)
Output	Level MIXED @Delay 0 Impedance	−20dBm (−3dBm max.) −35dBm (−18dBm max.) 570Ω @−20dBm, MIXED 1.8kΩ @−20dBm, DELAY 100Ω @−35dBm, MIXED 330Ω @−35dBm, DELAY	+4dBm (+17dBm max.) −20dBm (−5dBm max.) 100Ω @+4dBm 650Ω @−20dBm, MIXED 650Ω @−20dBm, DELAY
Feedback	Send Return	———	Level: +4dBm (17dBm max.) Impedance: 100Ω Level: +4dBm (17dBm max.) Impedance: 42kΩ
CV	In Inv Out	———	Operation Voltage: 0–10V Impedance: 100kΩ Level: 0–10V (⋀ wave) Impedance: 1kΩ
General Performance	Delay Time (millisec) TIME X2 Off TIME X2 On	0–375–562 (X1.5) 0–750–1125 (X1.5)	0–1500–2250 (X1.5) 0–3000–4500 (X1.5)
		0.1ms steps (0–10ms) 1ms steps (10ms-max.)	
	Delay Accuracy	±0.4%	
	Frequency Response	10Hz–100kHz 0, −1dB @Direct 10Hz–17kHz +0.5, −3dB @Delay, 0–375ms 10Hz–8.0kHz +0.5, −3dB @Delay, 0–1125ms	10Hz–100kHz +0, −1dB @Direct 10Hz–17kHz +0.5, −3dB @Delay, 0–1500ms 10Hz–8kHz +0.5, −3dB @Delay, 0–4500ms
	Signal to Noise Ratio (IHF A) at rated input & output	90dB Direct 80dB, Delay	90dB, Direct 88dB, Delay
	Dynamic Range	Greater than 112dB, Direct Greater than 90dB, Delay	Greater than 112dB, Direct Greater than 100dB, Delay
	Total Harmonic Distortion at rated input & output Ref. 1kHz	Less than 0.05% Direct 0.08% typ 0.2% max, Delay	Less than 0.008% typ Direct 0.03% typ Delay
Power Consumption		17W	24W
Dimensions	482(W) x 46(H) x 310(D) mm 19(W) x 1-13/16(H) x 12-13/16(D) in		
Weight	5kg / 11 lb		

0/3000 ES lition

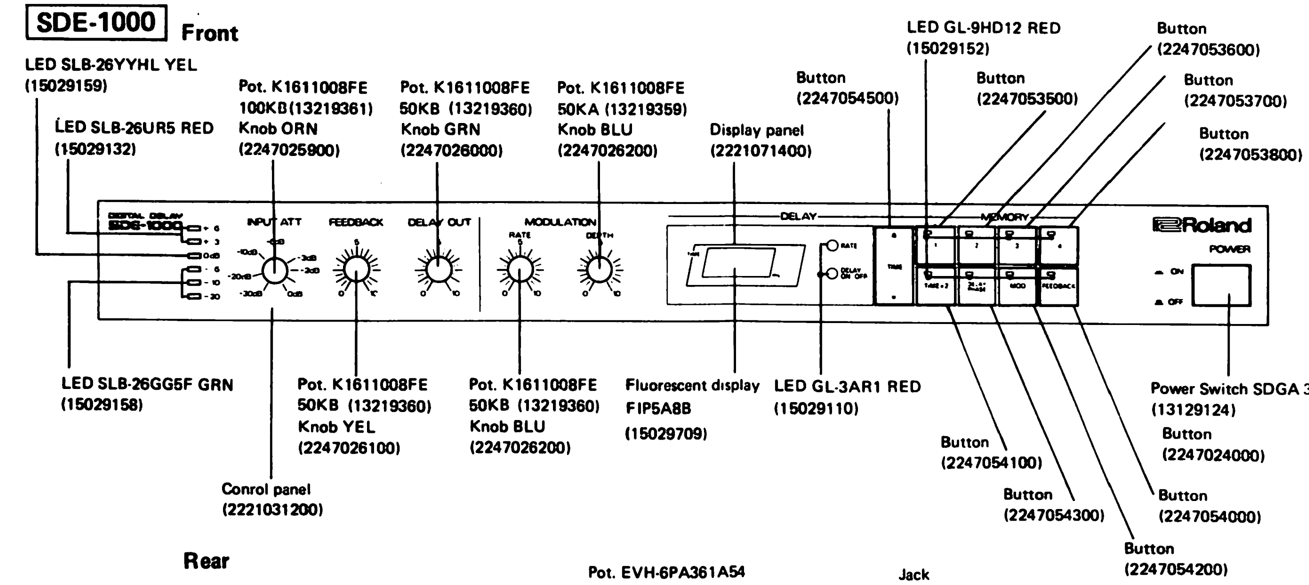
SDE-3000 Front



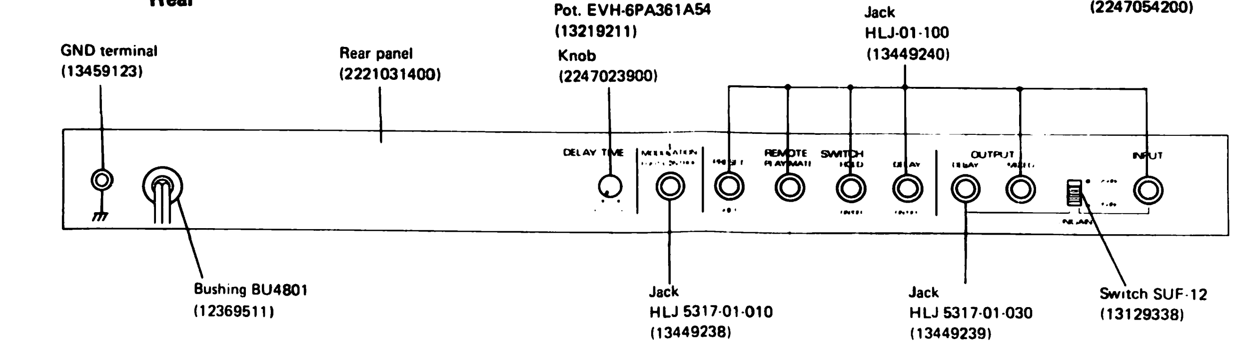
Rear



SDE-1000 Front

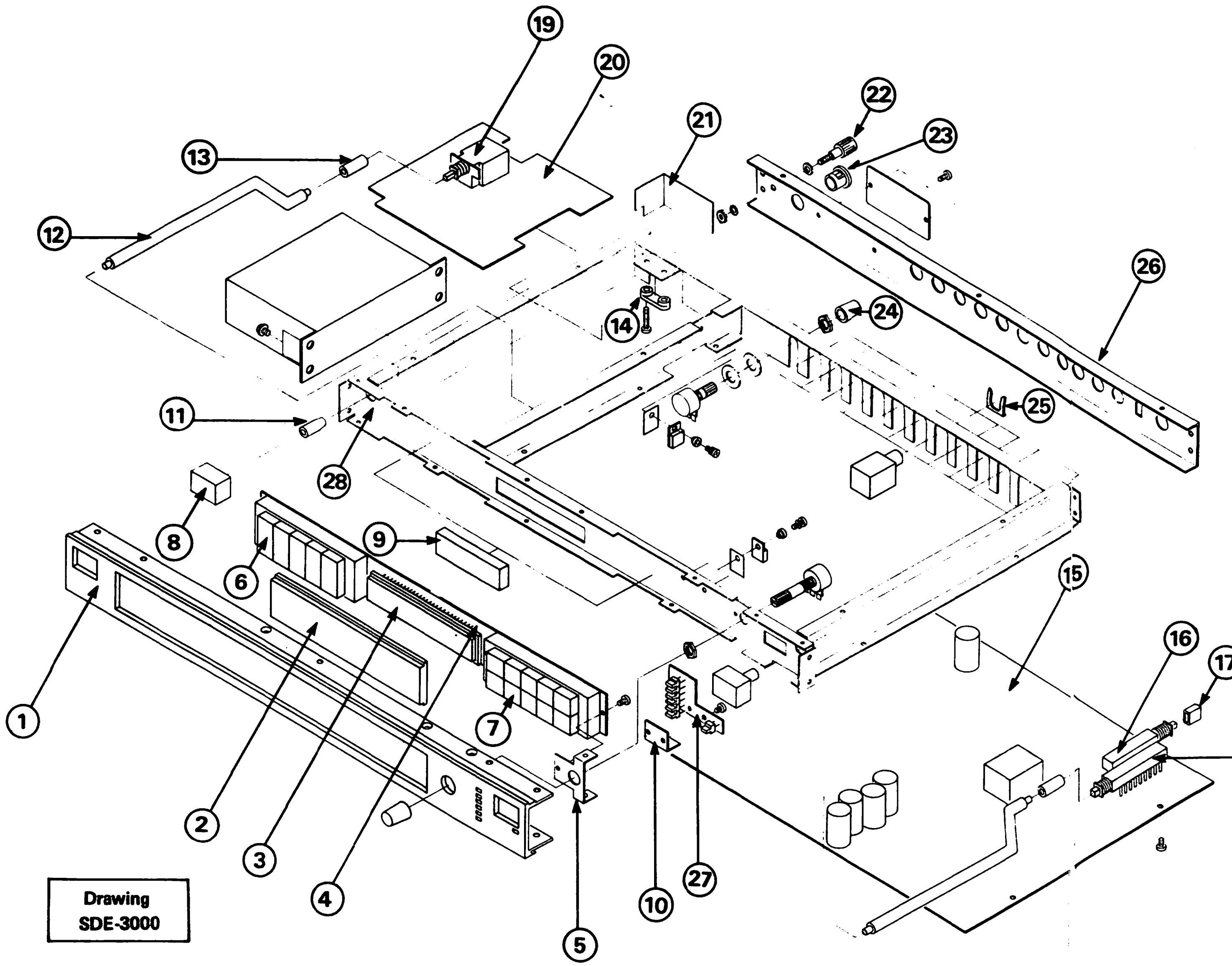


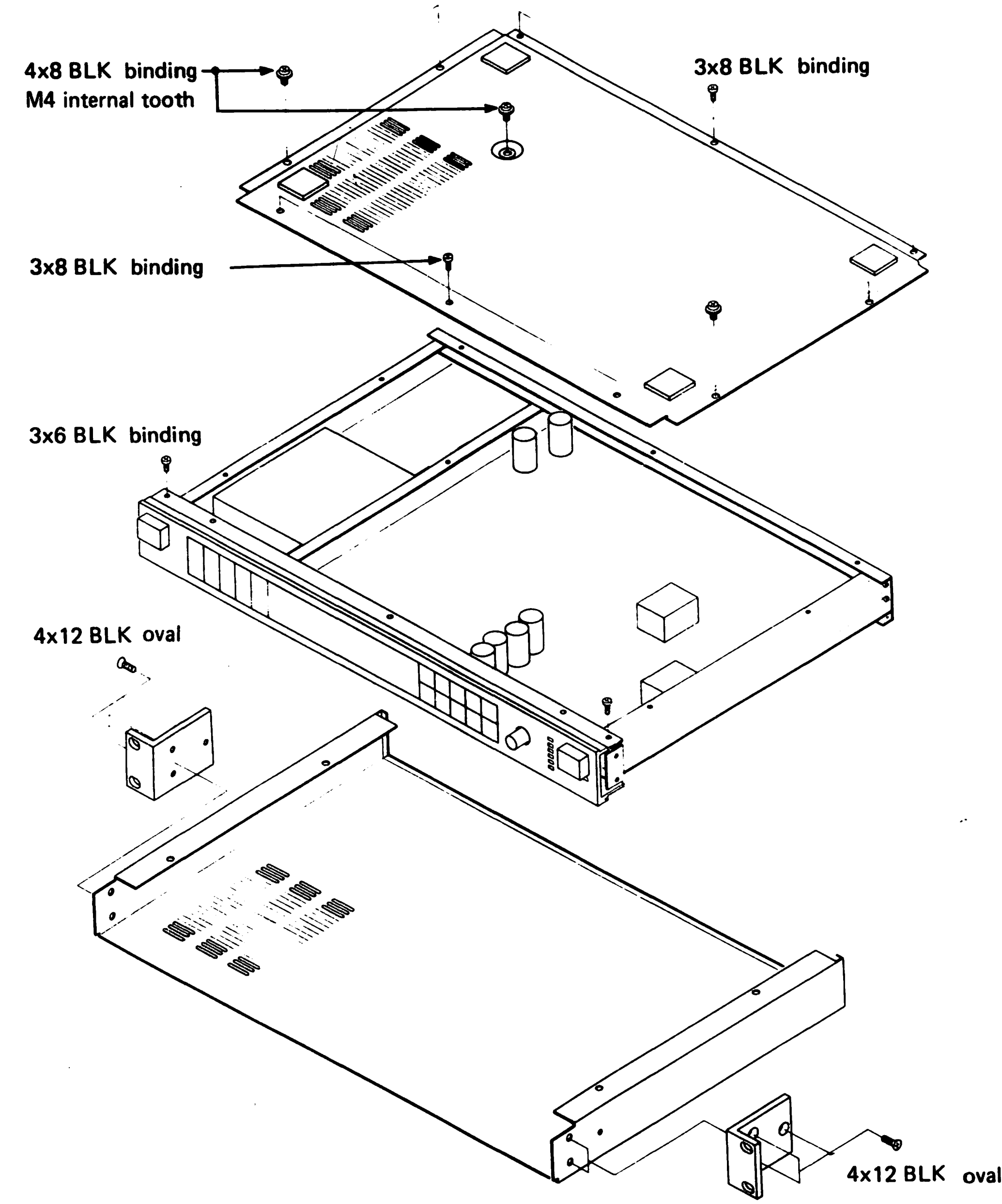
Rear



EXPLODED VIEW

SDE-1000/3000





(1000): SDE-1000, (3000): SDE-3000

- (1)--Control panel
  - 2221031200 (1000)
  - 2221031100 (3000)
- (2)--Display panel
  - 2221071400 (1000)
  - 2221071300 (3000)
- (3)--Fluorescent display
  - 15029709 FIP5A8B (1000)
  - 15029710 FIP16A5R (3000)
- (4)--Switch board
  - 7411608005 (1000)
  - 7411708005 (3000)
- (5)--PCB holder
  - 2219031801
- (6)--Button assembly
  - 2247090300 (1000)
  - 2247090100 (3000)
- (7)--Button assembly
  - 2247090200 (3000)
- (8)--Button BLK
  - 2247024000
- (9)--Cushion
  - 2226022200
- (10)--LED holder
  - 2219031900
- (11)--Joint A
  - 2215040100
- (12)--Connection rod
  - 2214020700
- (13)--Joint B
  - 2215040200
- (14)--Line cord strain relief
  - 12369410 1702B
- (15)--Main board
  - 7411606032 (1000)
  - 7411706026 (3000)
- (16)--Push switch
  - 13129338 SUF-12
- (17)--Button WHT
  - 12470514
- (18)--Push switch
  - 13129337 SUE-12 (3000)
- (19)--Push switch
  - 13129124 SDGA 3P
- (20)--Power board
  - 7411609000 (1000)
  - 7411709000 (3000)
- (21)--Insulation sheet
  - 2216052701
- (22)--GND terminal
  - 13459123
- (23)--Bushing
  - 12369511 BU4801
- (24)--Knob 10mm dia.
  - 2247023900
- (25)--Snap pin
- (26)--Rear panel
  - 2221031400 (1000)
  - 2221031300 (3000)
- (27)--LED board
  - 7411607001 (1000)
  - 7411707001 (3000)
- (28)--Chassis
  - 2281032001 (1000)
  - 2281031901 (3000)

PARTS LIST

CASE

2202020500	Bottom cover	
2219031801	PCB holder	
2219031900	LED holder	
2219032000	Switch holder	
2212050900	Rack angle	
2221031200	Control panel	(SDE-1000)
2221031400	Rear panel	(SDE-1000)
2202022903	Top cover	(SDE-1000)
2281032001	Chassis	(SDE-1000)
2221071400	Display panel	(SDE-1000)
2221031100	Control panel	(SDE-3000)
2221031300	Rear panel	(SDE-3000)
2202020403	Top cover	(SDE-3000)
2281031901	Chassis	(SDE-3000)
2221071300	Display panel	(SDE-3000)
15029709	Fluorescent display FIP5A8B	(SDE-1000)
15029710	Fluorescent display FIP16A5R	(SDE-3000)

KNOB, BUTTON

2247023900	Knob 10mm dia.	
2247025900	Knob ORN	
2247026000	Knob GRN	(SDE-1000)
2247026100	Knob YEL	(SDE-1000)
2247026200	Knob BLU	(SDE-1000)
12470514	Button WHT	
2247024000	Button BLK	
2247090300	Button Assembly (includes the following)	(SDE-1000)
2219032000	Switch holder	
2247053500	Button 1	
2247053600	Button 2	
2247053700	Button 3	
2247053800	Button 4	
2247054000	Button FEEDBACK	(SDE-1000)
2247054100	Button TIME X2	
2247054200	Button MOD	
2247054300	Button DELAY PHASE	
2247054500	Button TIME	
2247090200	Button Assembly (includes the following)	(SDE-3000)
2219032000	Switch holder	
2247053400	Button BANK A/B	
2247053500	Button 1	
2247053600	Button 2	
2247053700	Button 3	
2247053800	Button 4	
2247053900	Button FILTER	(SDE-3000)
2247057700	Button FEEDBACK PHASE	(SDE-3000)
2247054100	Button TIME X2	
2247054200	Button MOD	
2247054300	Button DELAY PHASE	
2247090100	Button Assembly (includes the following)	(SDE-3000)
2219032000	Switch holder	
2247054400	Button FEEDBACK	(SDE-3000)
2247054500	Button TIME	
2247054600	Button DEPTH	(SDE-3000)
2247054700	Button OUT	(SDE-3000)
2247054800	Button RATE	(SDE-3000)

SWITCH

13129338	SUF-12		
13169621	KEF 10906		
13129124	SDGA 3P		
13129337	SUE-12		(SDE-3000)
12439206	PRBD-4	reed relay	(SDE-3000)

JACK

13449238	HLJ5317-01-010
13449239	HLJ5317-01-030
13449240	HLJ5317-01-100

TRANSFORMER

22450348N0	100/117V	(SDE-1000)
22450349D0	220/240V	(SDE-1000)
22450350N0	100/117V	(SDE-3000)
22450351D0	220/240V	(SDE-3000)

COIL

2244023800	LPF S097624	
2244023900	LPF S097623	
12449236	OSC S097614 L1	(SDE-3000)

PCB

7411606032	Main board	(pcb 2291058201)	(SDE-1000)
7411607001	LED board	(pcb 2291058300)	(SDE-1000)
7411608005	Switch board	(pcb 2291058400)	(SDE-1000)
7411706026	Main board	(pcb 2291057901)	(SDE-3000)
7411707001	LED board	(pcb 2291058000)	(SDE-3000)
7411708005	Switch board	(pcb 2291058100)	(SDE-3000)
7411709000	Power supply board	(pcb 2291058500)	
	Fuses, Fuse labels, capacitor C1 excluded. Specify model and line voltage when ordering for complete assy.		
7411711002	RAM board	(pcb 2291083800)	(SDE-3000)
----------	Analog SW board	(pcb 2291091900)	
	Substitutive for HI-302 and HI-303. No replaceable part. See P.20.		

POTENTIOMETER

13219361	K1611008FE 100KB	
13299101	EVT-R4SA00B14	trimmer

13299102	EVT-R4SA00B15	trimmer	
13219359	K1611008FE 50KA		(SDE-1000)
13219360	K1611008FE 50KB		(SDE-1000)
13219211	EVH-6PA361A54		(SDE-1000)
13299111	H1051A009 2.2KB	trimmer	(SDE-1000)
13299107	EVT-R4SA00B54	trimmer	(SDE-1000)
13219214	EVH-6PA361B54		(SDE-3000)
13299109	H1051A007 1KB	trimmer	(SDE-3000)
13299113	H1051A011-4R7KB	trimmer	(SDE-3000)

FUSE

12559105	SGA	1A	100/117V	
12559510	CEE	T400mA	220/240V	
12559504	CEE	T100mA	220/240V	(SDE-1000)
12559506	CEE	T160mA	220/240V	(SDE-3000)

IC

15229811	MB63H101	Gate array (Main Controller)	
15179141	MSM80C49-44RS	CPU	
15179315	M5K4164NP-20	64K D-RAM	
15159702	M54563	Transistor array	
15169355	SN74LS48N	7-Segments decoder	
15159101H0	HD14001 BP	Quad 2 Input NOR	
15159104H0	HD14011 BP	Quad 2 Input NAND	
15159112H0	HD14049 BP	Inverter	
15159133	HD14174 BP	Dual D-Flip-Flop	
15189111J1	NJM311D	Comparators	
15189163	MB3761M	Voltage detector	
15219116	IR2E02	LED Driver	
15189136	M5218L	OP Amp	
15189141	NJM4562DD	OP Amp	
15199106F0	µA7805UC	Three Terminal Voltage Regulator	
15169102H0	HD7406P	Hex O.C. Inverters	(SDE-1000)
15169117H0	HD7407P	Hex O.C. Buffers	(SDE-1000)
15169356	SN74LS628N	VCO	(SDE-1000)
15219108	NE570N	Compandor	(SDE-1000)
15189152	NJM5534D	OP AMP	(SDE-1000)
15159115H0	HD14066 BP	Analog Switch	(SDE-1000)
1599104F0	µA7812 UC	Three Terminal Voltage Regulator	(SDE-1000)
15169301H0	HD74LS00	Quad 2 Input NAND	(SDE-3000)
15169311H0	HD74LS74P	Dual D-Flip-Flop	(SDE-3000)
15169332H0	HD74LS157P	2 to 1 Data Selectors	(SDE-3000)
15169357	74LS283	4 bit Binary Full Adders	(SDE-3000)
15159105H0	HD14013 BP	Dual D-Flip-Flop	(SDE-3000)
15159129H0	HD14053 BP	Triple 2-channel Multiplexer	(SDE-3000)
15189160	TDB0119	Dual Voltage Comparator	(SDE-3000)
15219120	AM6012	D/A Converter	(SDE-3000)
15159513	HI-201-5	Quad Analog Switch	(SDE-3000)
15159523	HI-302-5	Dual Analog Switch	(SDE-3000)
15159522	HI-303-5	Dual Analog Switch	(SDE-3000)
15189161	HA-2525-5	OP Amp	(SDE-3000)
15189118J0	NJM082DR	OP Amp	(SDE-3000)
15229802	BA662 A	VCA	(SDE-3000)
15159316	TC4514 BP	4 to 16 Line Decoder	(SDE-3000)

TRANSISTOR

15119701	2SA968-Y	
15119125	2SA1115-F	
15129130	2SC1583-F	
15129704	2SC2238-Y	
15129137	2SC2603-F	
15129602	2SD667-C	
15129118	2SC1923-R	(SDE-3000)

FET

15139103	2SK30ATM-GR	
15139106	2SK117-GR	
15139108	2SK150-GR	(SDE-3000)

DIODE

15019125	1SS-133		
15019251	1N4007		
15019236	W-02	Rectifier Bridge	
15019525	RD5.6EB-2	Zener	
15029132	SLB-26UR5	LED RED	
15029159	SLB-26YYHL	LED YEL	
15029158	SLB-26GG5F	LED GRN	
15029152	GL-9HD12	LED RED	
15029110	GL-3AR1	LED RED	
15019103	1S-2473		
15019557	RD15EB-3	Zener	(SDE-1000)
15019209T0	S5500G		(SDE-3000)
15029148	GL-9ND2	LED RED/GRN	(SDE-3000)
15029111	GL-3PG1	LED GRN	(SDE-3000)
150192490X	KV1226X or KV1226Y (150192490Y)	Varicap	(SDE-3000)

RESISTOR

13919121	RNSA09P-473	47K x 8 array	
13769155D0	CRB25FX 1.8K	1/4W 1% 100PPM Metal oxide	
13769227D0	CRB25FX 5K	1/4W 1% 100PPM Metal oxide	
13769228D0	CRB25FX 7K	1/4W 1% 100PPM Metal oxide	
13769173D0	CRB25FX 10K	1/4W 1% 100PPM Metal oxide	
13769177D0	CRB25FX 15K	1/4W 1% 100PPM Metal oxide	
13919134	RKM14L492/103F	Network	(SDE-1000)
13919137	RNSA-09P272	27K x 8 array	(SDE-1000)
13910103	RNSA-09P103	10K x 8 array	(SDE-3000)
13919118	RGSD-16L104G	Ladder network	(SDE-3000)
13769121D0	CRB25FX 68	1/4W 1% 100PPM Metal oxide	(SDE-3000)
13769127D0	CRB25FX 120	1/4W 1% 100PPM Metal oxide	(SDE-3000)
13769131D0	CRB25FX 180	1/4W 1% 100PPM Metal oxide	(SDE-3000)
13769136D0	CRB25FX 300	1/4W 1% 100PPM Metal oxide	(SDE-3000)
13769151D0	CRB25FX 1.2K	1/4W 1% 100PPM Metal oxide	(SDE-3000)
13769153D0	CRB25FX 1.5K	1/4W 1% 100PPM Metal oxide	(SDE-3000)
15229909	ERS-B33G561	Posistor	(SDE-3000)

CAPACITOR

13549884M0	ECQM-6103MZ	0.01μF	100V	Polypropylene
13589455M0	ECQ-U2A103MF	0.01μF	220/240V	Polypropylene
13589456M0	ECQ-U1A103MC	0.01μF	117V	Polypropylene
13639154M0	ECEA1CS102	1000μF/16V		Electro
13639194M0	ECEA1VS102	1000μF/35V		Electro
13639923M0	ECEA1CN470S	47μF/16V		Bi-polar, electro
13589139Y0	YM92PS122-2A	0.0012μF		Polypropylene ±1% (SDE-1000)
13589140Y0	YM92PS152-2A	0.0015μF		Polypropylene ±1% (SDE-1000)
13619703NA	CS15E1VR22K1S	0.22μFx2		A set of pair, selected (SDE-1000)
13589138Y0	YM92PS102-2A	0.001μF		Polypropylene ±1% (SDE-3000)
13619711N0	CS15E1V4R7K1S	4.7μF/35V		Tantalum bead (SDE-3000)
13639155M0	ECEA1CS222	2200μF/16V		Electro (SDE-3000)
13639213M0	ECEA1HS471	470μF/50V		Electro (SDE-3000)
13639922M0	ECEA1CN100S	10μF/16V		Bi-polar, electro (SDE-3000)

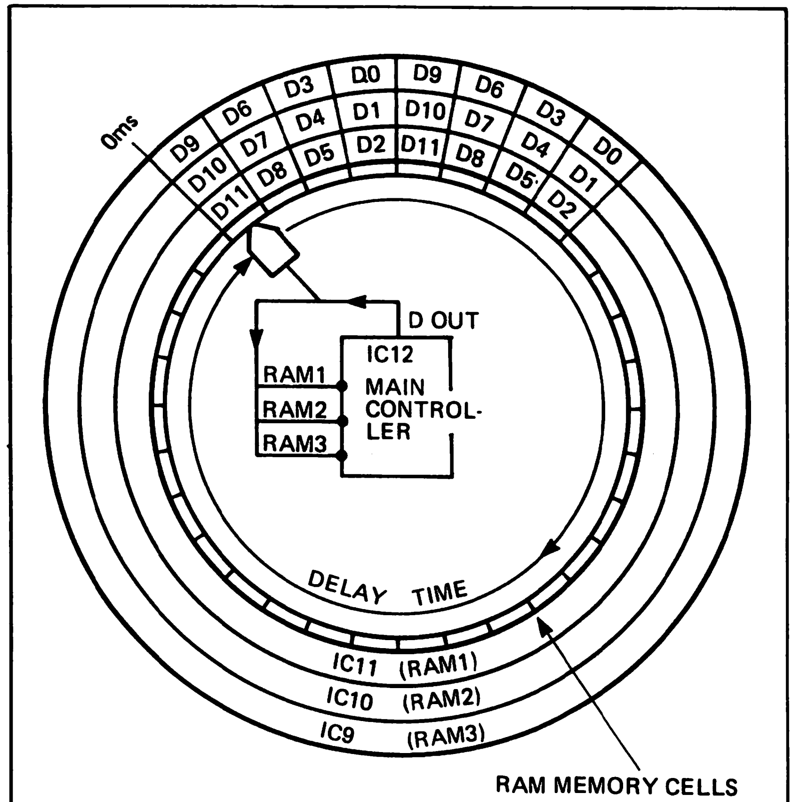
OTHERS

12389718	PX-1 11.0MHz Xtal		
2216031201	Insulation spacer (vinyl sheet)		
2216052701	Insulation sheet (fibre, L-shaped)		
2214020700	Connection rod		
2215040100	Joint A		
2215040200	Joint B		
13439127	Connector housing 5045-11A 11P		
13439157	Connector housing 5045-13A 13P		
2341043200	Connector wiring assy 11P		
2341043300	Connector wiring assy 13P		
12569111	CR1/3N 3V Lithium Battery		
2226022200	Cushion		
2225021001	Shield board (metal, L-shaped)		
2225021100	Shield board (metal, flat)		(SDE-1000)
2225011200	Shield sheet (foiled paper)		(SDE-1000)
2216031300	Insulation spacer (vinyl chloride)		(SDE-1000)
13439120	Connector housing 5045-04A 4P		(SDE-1000)
13439123	Connector housing 5045-07A 7P		(SDE-1000)
13429143	Connector housing EMC-S0760 7P		(SDE-1000)
2341017100	Connector wiring assy 4P		(SDE-1000)
2341018000	Connector wiring assy 7P	PS board	(SDE-1000)
2341030700	Connector wiring assy 7P	LED board	(SDE-1000)
2225021501	Shield board (metal, U-shaped)		(SDE-3000)
13439125	Connector housing 5045-090A 9A		(SDE-3000)
13429145	Connector housing EMCS0960 9P		(SDE-3000)
2341043400	Connector wiring assy 9P	SW board	(SDE-3000)
2341030300	Connector wiring assy 9P	LED board	(SDE-3000)
13439514	Connector PS-30 SD-S4TS1-1 30P female		(SDE-3000)
13439516	Connector PS-30 PA-S4T1-A1 30P male		(SDE-3000)
2215050900	Spacer 13mmL HEX threaded		(SDE-3000)
13459123	GND terminal		
12369511	Cord bushing BU4801		
12369410	Line cord strain relief 1702B		

CIRCUIT DESCRIPTIONS

General Description

SDE-1000/3000, Digital Delay Line, use RAMs as memory device in which audio signals are stored by means of PCM (Pulse Coded Modulation) method. The delay unit first samples the input audio signal to have a series of discrete values of the signal amplitude at point.
Each of sampled pulses is digitalized and stored into RAM cells as a binary coded data which, when a specified time passed, is read, restored to analog value, then injected into audio path as a delayed signal. The process can well be compared to that of conventional tape echo machine as shown in Fig. 1.
RAM cells correspond to the tape and the RAM accessing to a Record/Playback head.
In operation R/P head first functions as a playback head and will read a group of RAM cells being in touch with, then quickly changes to a recording head to record digital data being fed from the A/D converter into the same cells. The head steps to the next cell group and repeats the read and write operations, then to the third, fourth and so on continuously until the time determined by DELAY TIME button comes. When the delay time has passed, the head leaves the remaining cells unused and jumps to the first cell group where it reads the previously stored data and writes the new data. The number of cell groups the head can see is based on DELAY TIME setting and the travelling speed of the head slows down one-half when in TIME X2 mode. In other words, the length of the tape varies with Delay Time and the speed with Delay Time Range (also X1—X1.5 setting and MOD rate).
The following description breaks major circuits down into Analog and Digital, starting with SDE-1000 circuits most of which are also found in SDE-3000, then goes through the circuits featuring SDE-3000. One major difference between two models are their time delay ranges: SDE-3000 four times the SDE-1000 in RAM memory capacity.



SDE-1000
See P.13 for SDE-3000
Fig. 1

HEAD AMP

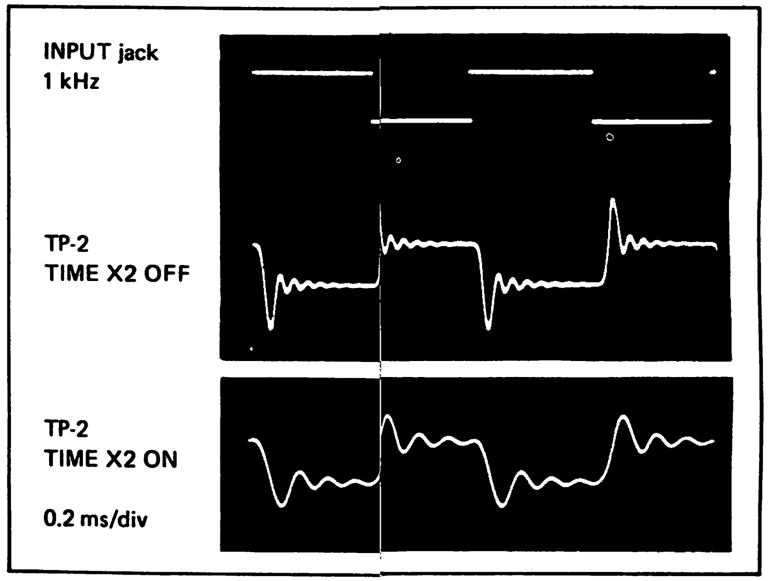
The Head Amp interfaces the unit wih a variety of input signals so that the unit can operate with adequate signal ɔ noise and without execessive limiting across the dynamic range of the signa Although this amp has a gain range of 1 to 24, VR-6 (INPUT ATT) attenuats the delay signal as it is rotated from FCW position to CCW. The unit's overll gain is unity at FCW.
NOTE: Minor modifications are madeon SDE-1000 head amp and associated circuits to provide more headroom without sacrificing tonal quality and sound level. Refer to Engineering Chage in SDE-1000 section in this manual.

FEEDBACK/MIXING

The delay signal is mixed again with new direct signal when 0V is placed on Q51 gate, and out of the delay line whn −14V is on the gate.

PREEMPHASIS

This stage boosts higher frequency corents to provide a good S/N ratio.
GAIN: unity at 1kHz and 2.5 at 10kH.



LPF-1

An *Anti-aliasing filter including tw filters of different cutoff point. Only one filter is connected to the next stge at a time. Pressing TIME X2 switch causes the Control Logic (IC14, etc to place a ground to the gate of Q27 and −14V to Q28, limiting the filtr's output bandwidth within 10Hz—8kHz. Disengaging the X2 switch corlucts Q28 and cuts off Q27, extending the bandwidth to 17kHz. Control Lgic also cuts off both FETs for 7 sec after power is first applied to the un; and during HOLD ON mode or while Delay Time button is manuplated.

*Aliasing — The type of distortioi that is found in "sampled" signal processing system when the signal has frquency components which exceed half the sampling frequency.

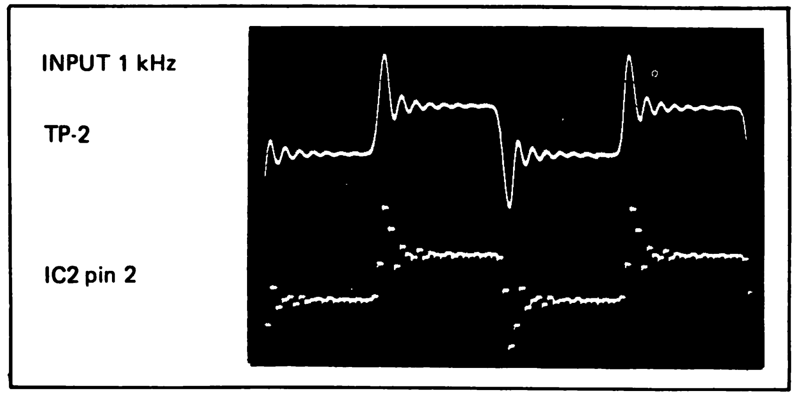
COMPRESSOR

This stage logarithmically reduces thedynamic range of the signal before it is digitalized.

NOTE: For detailed descriptions oi S/H, A/D, D/A, Main Controller and RAM, see corresponding sections in SDE-3000 description.

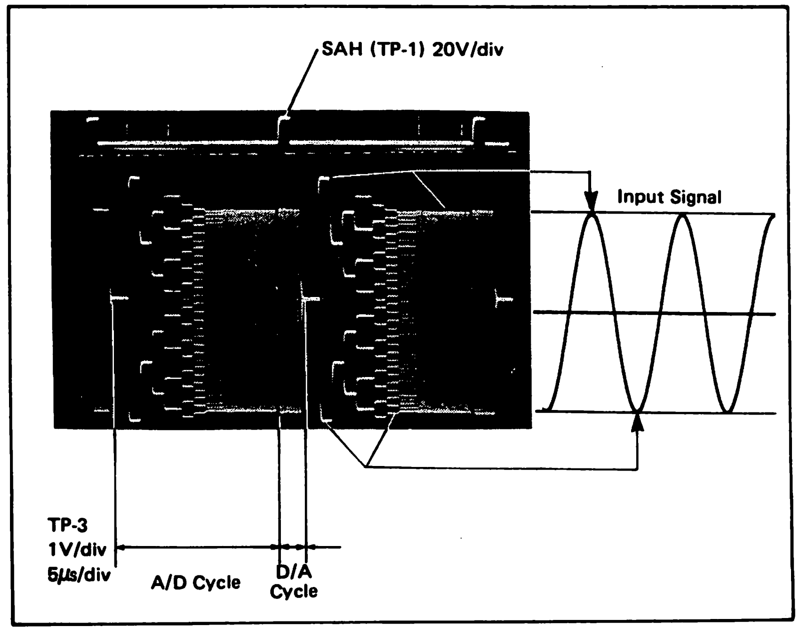
SAMPLE & HOLD

ICs 5A and 5B, together with C13 extract a portion of the input signal at SAH rate. The sampled audio is fed through Q8 to pin 2 of IC2 where it is compared with 12 step voltages on pin 3 to have its analog voltage represented by digital code through A/D conversion.
NOTE: SAH rate is constant regardless of DELAY TIME setting, but varies when TIME X2, DELAY TIME X1/X1.5 or MODULATION is enabled.



A/D CONVERTER

The A/D Converter employed here is of Successive Approximation consisting of SAR (Successive Approximation Registers in IC12, Main Controller), ICs 3 and 4 which boost TTL compatible to 12V, RM-1 ladder resistor which adds a corresponding analog weight to individual bit, Q9 and Q10 follower and comparator IC2.
In operation, SAR first sets the highest bit (MSB) register to H (1) whose output is, after given the highest voltage at RM-1, compared with sampled audio at IC2 input. If MSB is larger than the sampled audio, it is reset to L(0) by a H from IC2 (D IN).
If smaller, kept set and applied once more together with the second highest bit register output (H) that is one-half the highest in voltage. The process repeats for MSBs while the combination of SAR outputs is approaching to the sampled audio level. During the process, D IN is also transferred to RAMs IC9-IC11 to record H or L of all the bits which, when grouped into 12 bits, are the data of the sampled portion of audio input signal.



D/A CONVERTER

When the time determined by DELAY TIME has passed, some parts of A/D system serve as D/A converter. RAM stored 12-bit data is transferred in time sequence (3 bits parallel x 4 times) from each RAM OUT pin to IC12 where they are so arranged that they are fed simultaneously via D11-D10, ICs 3, 4, RM-1, Q9 and Q10 to S/H IC5C and IC5D.

EXPANDER

One half IC15 NE570 exponentially amplifies delayed audio to restore it to the original dynamic range.

LPF-2

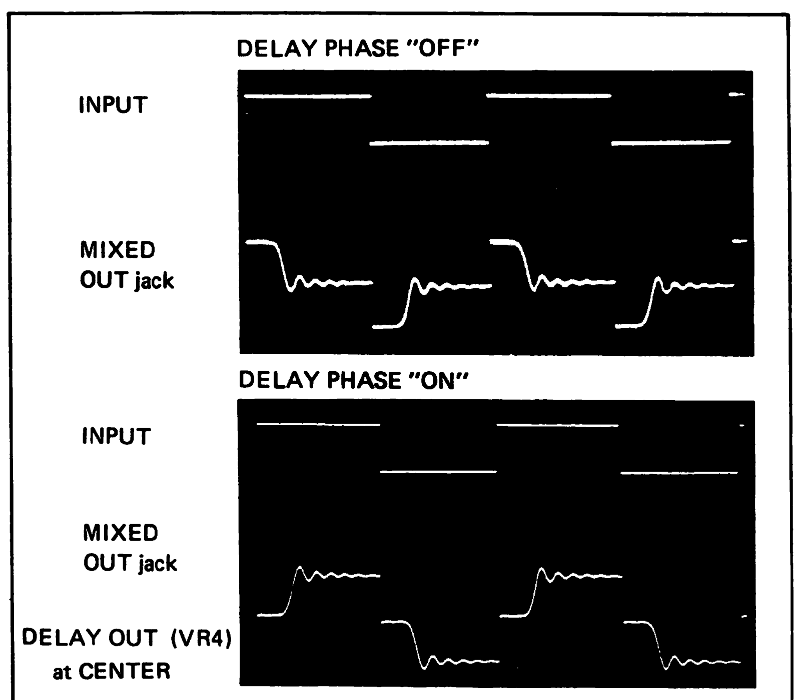
The configuration analogues to LPF-1, providing 19kHz bandwidth when Q48 is ON, or 9.5kHz when Q49 is selected by TIME X2 switch. Being an interporating filter, it smoothes staircase-like out of the waveform. As just for LPF-1, mute signals are applied from Control Logic IC14.

DE-EMPHASIS

IC29 and associated components reduce higher frequency components in the delay line to compensate for preemphasis, restoring the overall frequency response to flat.

PHASE SELECTOR

Q45, when conducted, change IC28 into an inverter, reversing the delay output phase with respect to the direct signal.



MAIN CONTROLLER

IC12 63H-101 a specially designed gate array for controlling digital delay system. It clocks most of delay related sequences such as A/D, D/A, S/H, RAM accessing, etc. in time with clocks generated at the internal timing generator which in turn is clocked on MSCK delivered from CLOCK Generator IC23. With TIME X2 button activated IC12 has an H on RNG 1 pin and slows down all timing sequences by one-half except REFRESH cycle. The clock frequency can be varied by the external voltages to be applied on FC pin or PA pin.

As the name implies, IC12 Main Controller is the heart of the Delay Line. All the delay circuits will not work correctly should the Main Controller fail to receive adequate clocks from IC23.

IC12 PIN DESCRIPTION

SAH & RNG 1

SAH determines the rate of sampling being performed at IC5 which gates on a high SAH. When TIME X2 is engaged, RNG 1 turns from L to H, lengthening SAH intervals from 22.9μs to 45.8μs.

D IN

D IN accepts a series of H or L from the comparator IC2, resetting register(s) in SAR on H to omit it from the subsequent comparisons.

D OUT

These Hs and Ls on D IN are also transferred to RAMs (IC9-IC11) and stored as a set of 12-bit data which represent the amplitude of a portion of input signal (sampled audio) being fed to IC2 pin 2.

D0—D11

During A/D conversion cycle these pins represent comparison data from internal SAR. During D/A cycle, simultaneously output 12-bit RAM stored data which have been read from each RAM in time sequence (3-bits x 4) and temporarily buffered in internal three registers.

DATA & SHIFT (SIFT)

As mentioned in general descriptio, RAM cells used for sound memory ae varied with time delay. IC12 contrls RAMs accessing sequence in accordance with DELAY TIME DATA received at SHIFT rate. The DATA is a serial stream of 16 bits and will change between:

┌—16 bits—┐
MSB LSB
0000 .... 000 at 0ms setting an
0011 .... 111 at maximum settg
↓
11 (SDE-3000)

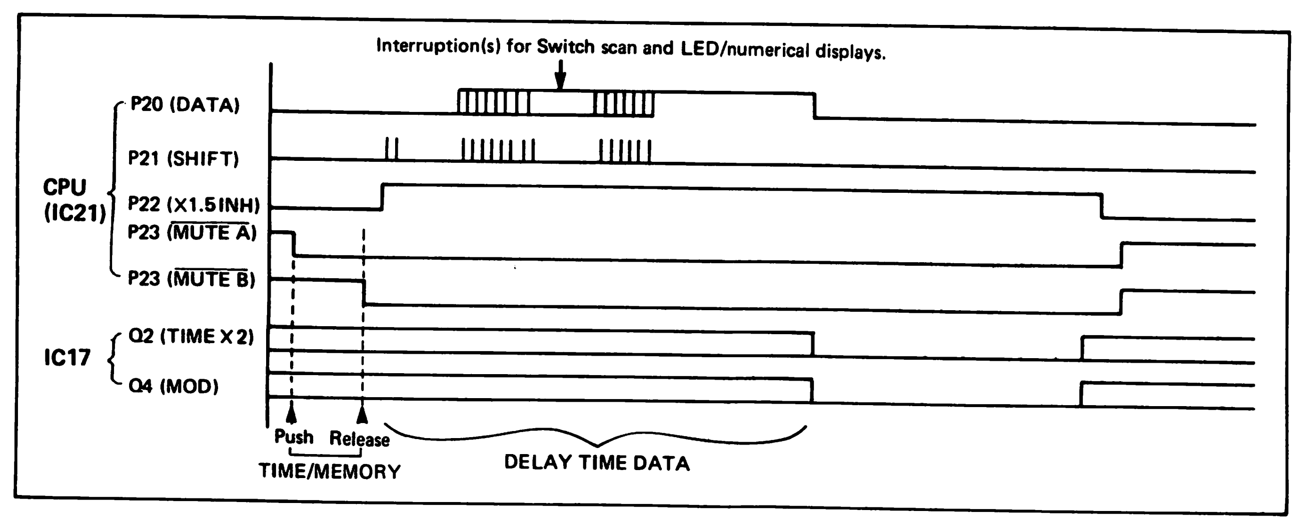
The DATA/SHIFT are transmittd only after DELAY TIME or PRESI button is released.

The DATA is accompanied by sevel mute signals to cancel unwantl signals.

MUTE A: active low when DEL/ TIME button is manplated.

MUTE B: active low while PRES is pressed.

To shorten the Mute periods, TIE X2, MOD., and X1.5 are disabled.



A0—A7

These pins feed RAMs with addresses: Refresh, Row and Column. Since the number of RAM cells involved in data storage is varied with DELAY TIME setting, the numbers of Row and Column addresses are also changed accordingly while Refresh addresses are issued for all the RAM cells.

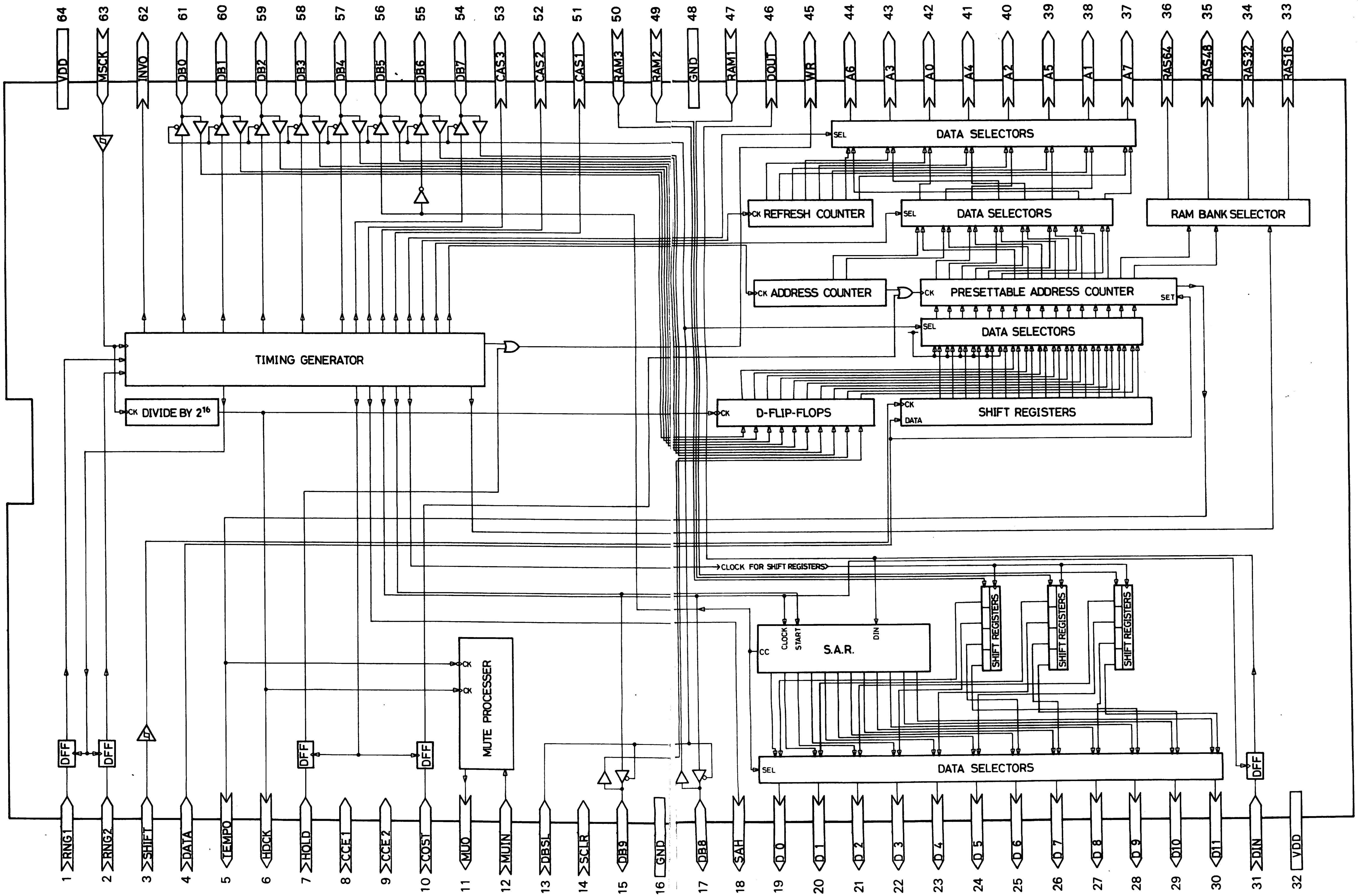
RS(RAS) 16

Falling edges of RAS (Row Address Strobe) enable each RAM to latch Row address (W/R cycle) or Refresh address into its designated cells.

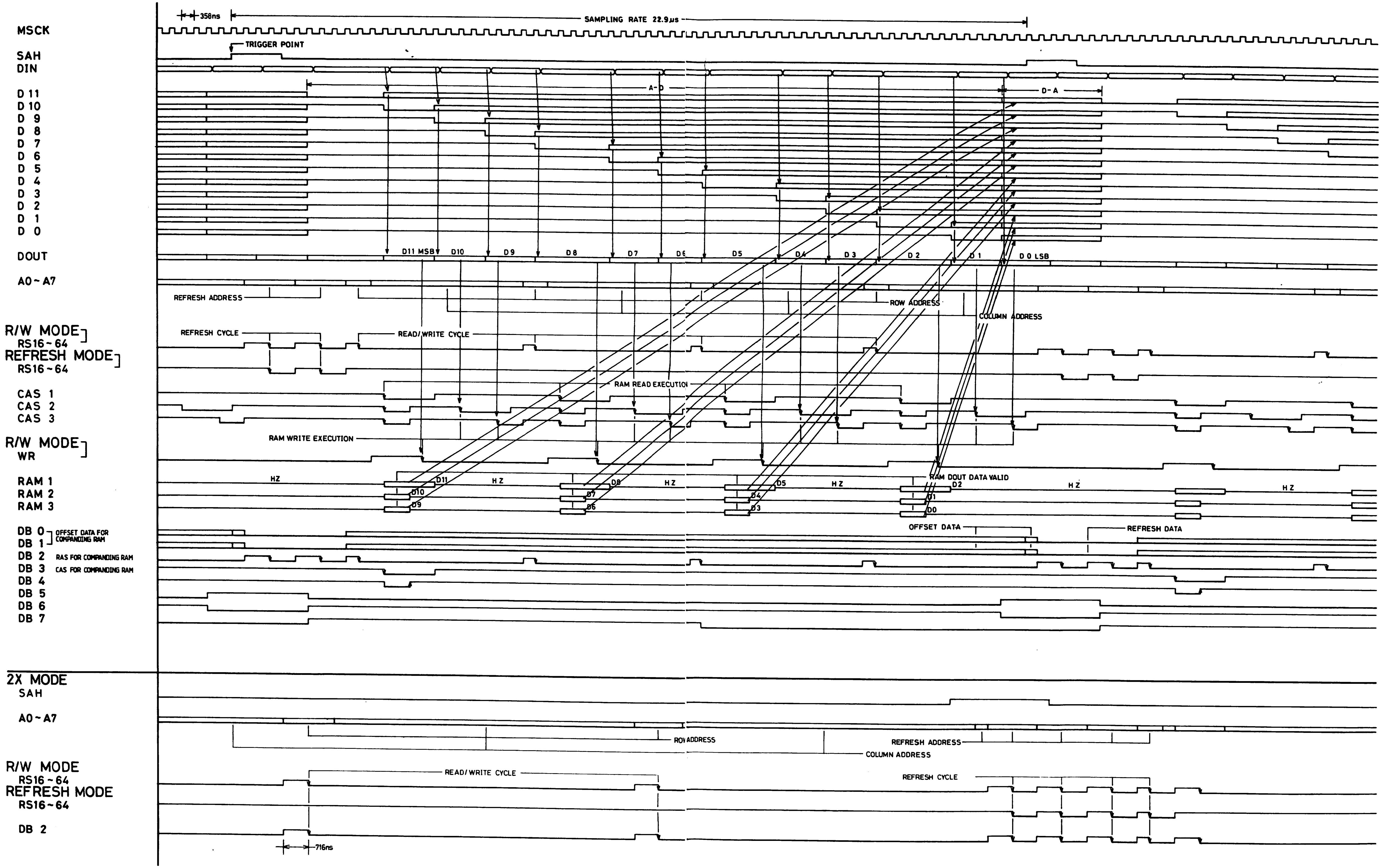
CAS 1—CAS 3

RAMs IC9—IC11 latch Column addresses on negative edges of cocurrent Column Address Strobes (CAS1CAS3) which also serve as Chip select, and read memory cell respectively. The data read are routed to the RAM D OUT (pin 14) while related CAS is low.

MAIN CONTROLLER BLOCK DIAGRAM
IC12 (SDE-1000)/IC31 (SDE-3000)



MAIN CONTROLLER TIMING DIAGRAM
IC12 (SDE-1000)/IC31 (SDE-3000)



MSCK, HDCK & CLOCK GENERATOR

The frequency of Clock Generator is as follows (approx):

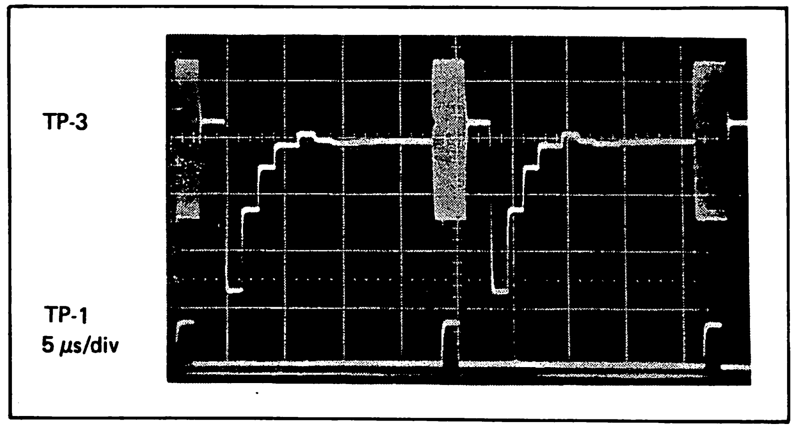
2.7MHz at Normal 1.7MHz at TIME X1.5
2.7M–3.3MHz at MOD max. 1.7M–2MHz at TIME X1.5/MOD max.

MSCK – Clocks the internal Timing Generator that times the most of digital circuits.

HDCK – The frequency of HDCK is MSCK or 43Hz at normal mode. Used by the CPU as a time base for calibrating Delay Time display. The CPU fails to read switches and jacks if HDCK period is outside 7m-50ms.

RAM 1–RAM 3

12-bit data read from three RAMs are fed through these pins to internal three shift registers for temporary storage. All the buffered bits are placed on D0-D11 at a time to form a 12-bit parallel data to be applied to D/A converter for reproducing a part of delay signal.
During HOLD ON the A/D converter remains active but cannot receive input signal. The comparator output is inhibited from being written into RAMs.



RAMs (IC9–IC11)

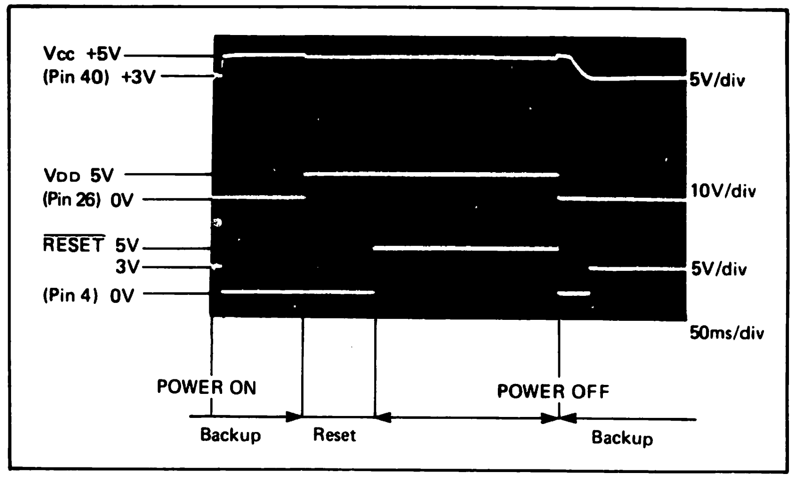
Record the results of Successive Approximation, from MSB (D11) to LSB (D0), sharing 12 bits – 4 specific bits for each as shown in the table at the beginning of General Description.

CONTROL SIGNALS IN DIFFERENT MODES

SDE-1000	IC21 P23	IC21 P14	x2 INDICATOR or IC17 Q2	FOOT SW JACK HOLD ON/OFF	FOOT SW JACK DELAY ON/OFF	DELAY ON/OFF LED(D4)	IC12 HOLD	A Q27 GATE	B Q28 GATE	C Q49 GATE	D Q49 GATE
Mute Mode	0	0	0	0	1	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0
	0	1	0	1	1	0	0	0	0	0	0
	0	1	0	1	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0
	0	1	1	1	1	0	0	0	0	0	0
	0	1	1	1	0	0	0	0	0	0	0
Normal Mode	1	0	0	0	1	0	0	0	1	0	0
	1	0	0	0	0	1	0	0	1	0	1
	1	1	0	1	1	0	1	0	0	0	0
	1	1	0	1	0	1	1	0	0	0	1
	1	0	1	0	1	0	0	1	0	0	0
	1	0	1	0	0	1	0	1	0	1	0
	1	1	1	1	1	0	1	0	0	0	0
	1	1	1	1	0	1	1	0	0	1	0
Remarks	0: 0V 1: 5V	0: 0V 1: 5V	0: 0V Indicator OFF 1: 5V Indicator ON	1: ON SW open 0: OFF SW closed or NOR-MAL	1: ON SW closed 0: OFF SW open or NOR-MAL	0: LED OFF 1: LED ON	0: 0V 1: 5V	0: –14V 1: 0V	0: –14V 1: 0V	0: –14V 1: 0V	0: –14V 1: 0V

CPU

The CPU is provided with a battery backup to retain switch, delay time and preset settings.



T0 – Decides the operation mode of the CPU:

+5V - - - SDE-1000
0V - - - SDE-3000

T1 – Receives Clock pulses through IC12 HDCK pin. The clock serves as a time base to enable the CPU to calibrate Delay Time Display and is ignored by the CPU when Modulation is ON and MOD Foot control jack disengaged. (See HDCK, Main Controller.)

P20 (DATA) – Send memory access control data after every delay time
P21 (SHIFT) – settings (see DATA/SHIFT, Main Controller).

P23 – Becomes "L" for muting. (See timing chart in DATA, SHIFT, Main Controller.)

P10, P11 – Read SW1–SW10 through the matrix in combination with P24–P27 and DB7.

P12 – Input from PRESET SHIFT jack. A rising edge of this input steps PRESET memory.

P13 – MODULATION FOOT CONTROL jack input. With MODULATION ON and this input at low, CPU ignores T1 input. For example, rotation of DELAY TIME X1-X1.5 does not change TIME display.

P14 – HOLD jack input. When H, readings of TIME UP or DOWN and PRESET memory are inhibited.

P15 – PLAY MATE jack input. Active rising edge.

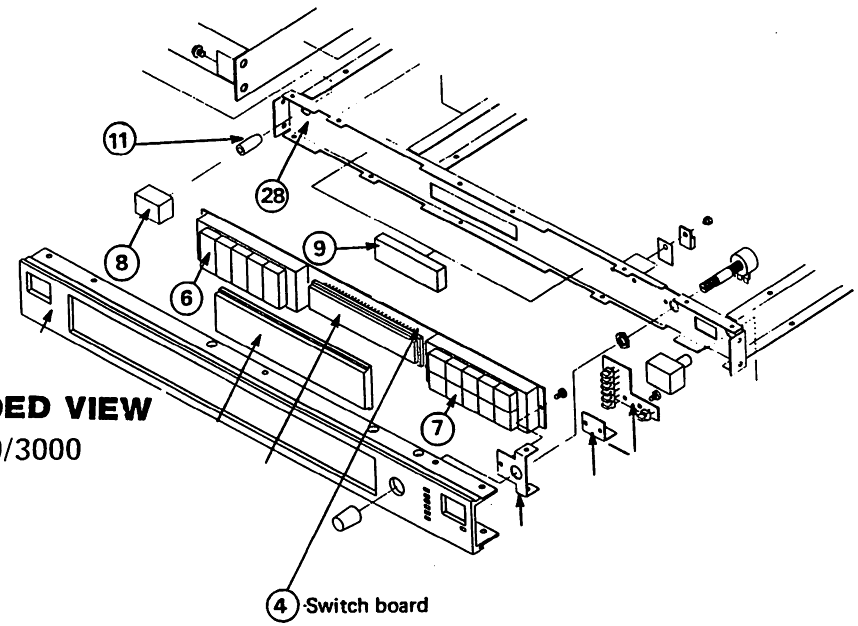
P16 – Rising edge from this pin latches the following logic codes made by DB0-DB3 into Analog Control IC17. TIME X2, DELAY PHASE, MOD and FEEDBACK

P24 – P27, DB7 – Output of switch scan signals which are read through P10 and P11.

DB0 – DB3 – Besides Control signals for IC17, these pins deliver numerical data to fluorescent display via IC18 7-seg-decoder. DB6: Dot Point signal.

DB4 – DB5 – Send LED lighting signals.

NOTE: When P10, P11, P12 and P15 pins receive signals almost at the same time, the CPU gives priority to the signal first read. Example: PRESET SHIFT and Front Panel switches are disabled when PLAY MATE has been activated.



EXPLODED VIEW
SDE-1000/3000

CORRECTION
PAGE 10

MSCK, HDCK & CLOCK GENERATOR

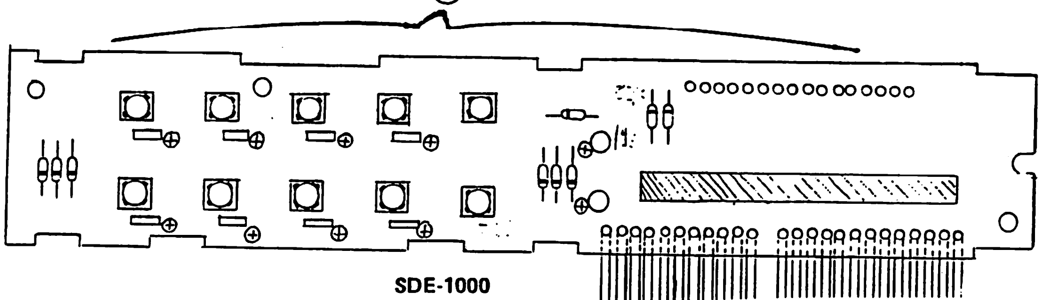
The frequency of Clock Generator is as follows (approx):

2.7MHz at Normal	1.7MHz at TIME X1.5
2.7M–3.3MHz at MOD max.	1.7M–2M

MSCK – Clocks the internal Timing Generato times the most of digital circuits.

HDCK – The frequency of HDCK is MSCK or 43Hz at normal mode. Used by the CPU as a time base for calibrating Delay Time display. The CPU fails to read switches and jacks if HDCK period is outside 7m-50ms.

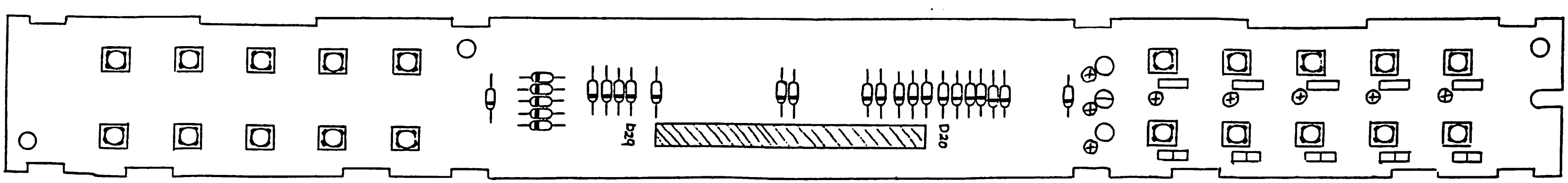
$\frac{MSCK}{2^{16}}$



SDE-1000
7411608005

Switch
KEF10906(13169621)

SDE-3000 7411708005



SDE-3000 DESCRIPTION

The following sections concentrate to the circuits particulár to SDE-3000. For other circuits not described, refer to those in SDE-1000.

HEAD AMP

Has a gain range of 2dB(1.26) to 30dB(31.6).

DELAY OUT/PHASE SELECT

This stage has 9.9dB gain. When TR78 is conducted, the delay out is 180° out of the direct signal.

MIXED OUT

Changes its gain with UNIGAIN settings:
7dB with UNIGAIN at +4dB
–3dB with UNIGAIN at –20dB

CV IN

Level shifts 0 to +12V inputs to ±4V.

INV OUT

Level shifts ±4V inputs to 0 to +12V.

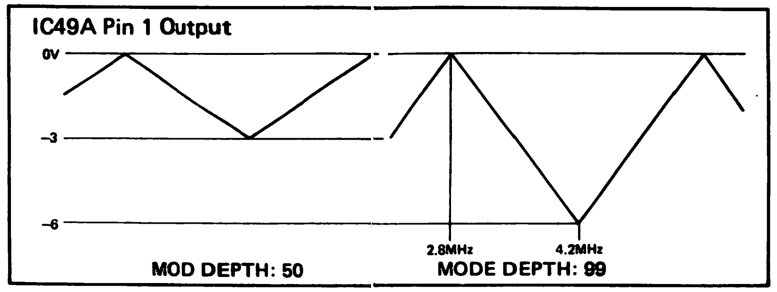
MOD DEPTH

Controls the amplitude of CV from CV IN or LFO with 0 to +5V coming via IC27A from RM8..

CV LINEARIZER

The output voltage at IC49A pin 1 is normally 0V.
Has a unique voltage response curve to compensate for nonlinear V/C characteristic of D62 varicap in VCO circuit.

MODULATION	X1–X1.5	IC49A Pin 1 (V)	VCO Frequency (MHz)
OFF	X1	0	2.8
ON (DEPTH MAX)	X1	0 to –6	2.8—4.2
OFF	X1.5	+2.8	1.84



IC31 MAIN CONTROLLER

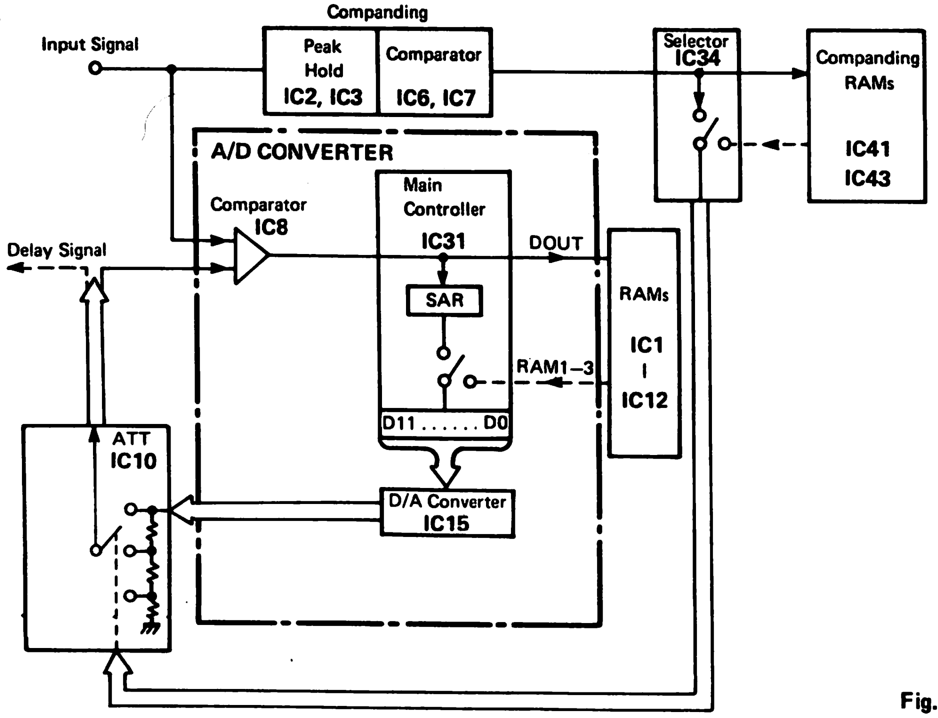
DB0, DB1 ------ Address offset data for companding RAMs. (See COMPANDING RAMs.)
DB4 -------------- Strobe . Latches data from companding RAMs into IC32 on rising edge.
DB5, DB6 ------ Signals D/A or A/D cycle.

Cycle	DB5	DB6
D/A	H	L
A/D	L	H

DATA COMPANDING

Audio signals are digitalized with a 12-bit Analog to Digital Converter before stored into RAM. In ordinary D/A conversion, the number of significant digits decreases as input signal level decreases, lowering relative resolution. The reason is well illustrated by comparing A/D system to a voltmeter.

Suppose the voltages ranging from IV to 100V are read with 100V scale, smaller voltages cannot be read accurately. The meter has to be switched down to lower ranges to allow the pointer stay around the middle of the scale. The same concept, named companding, is applied to SDE-3000 A/D conversion circuits.



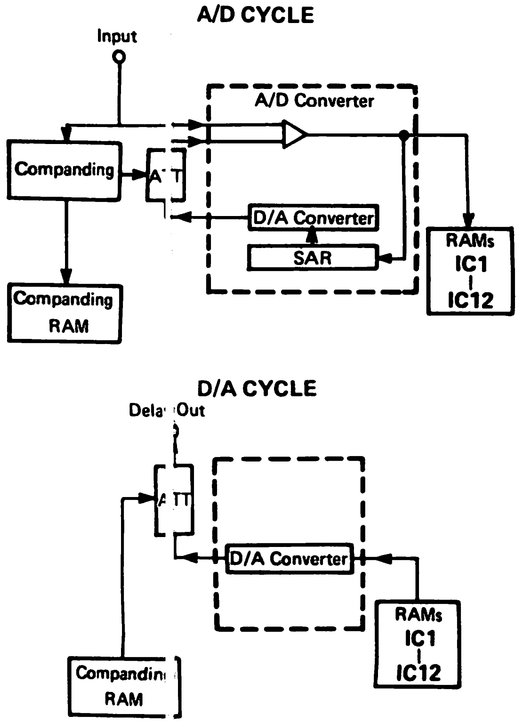
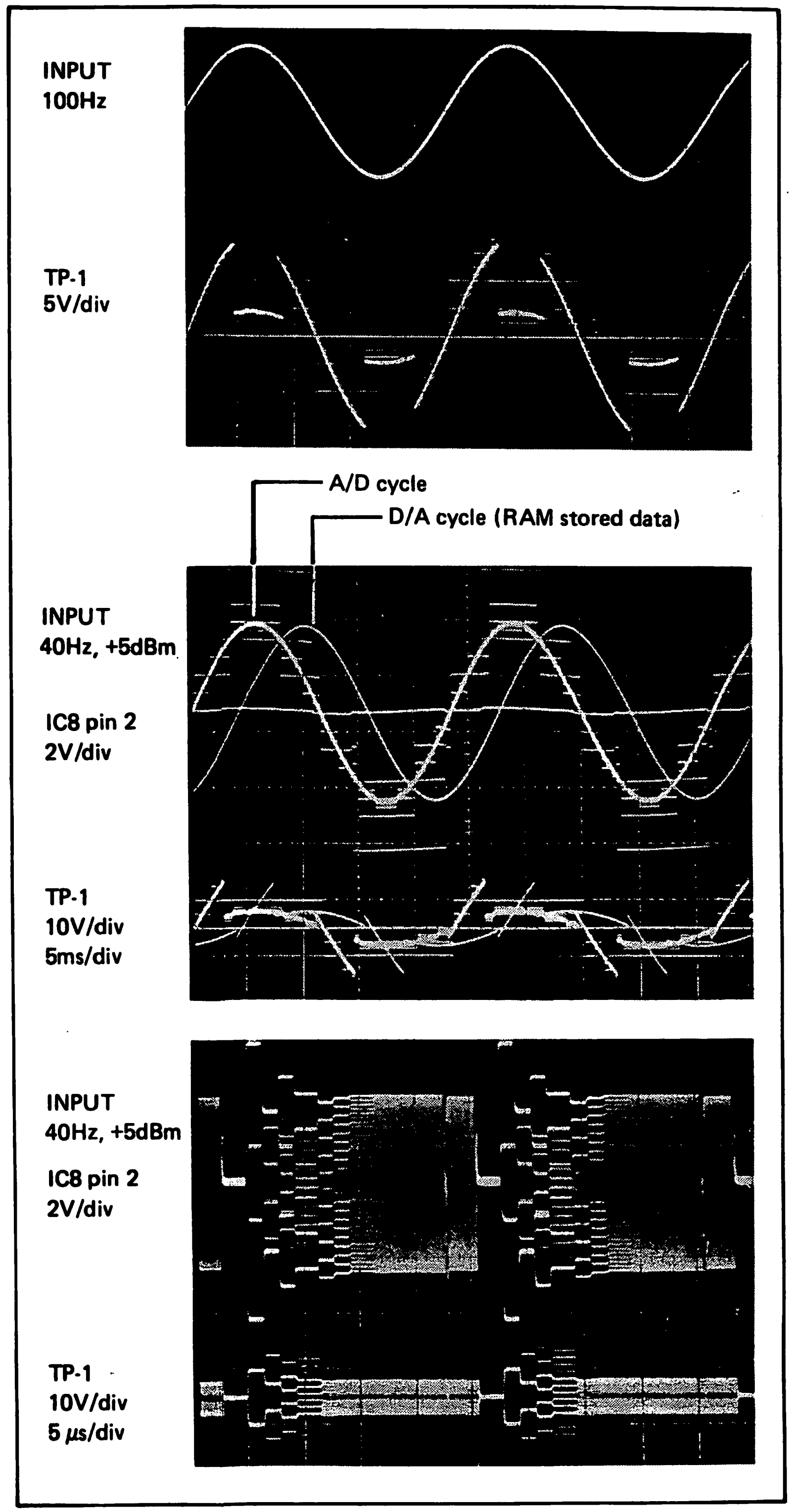


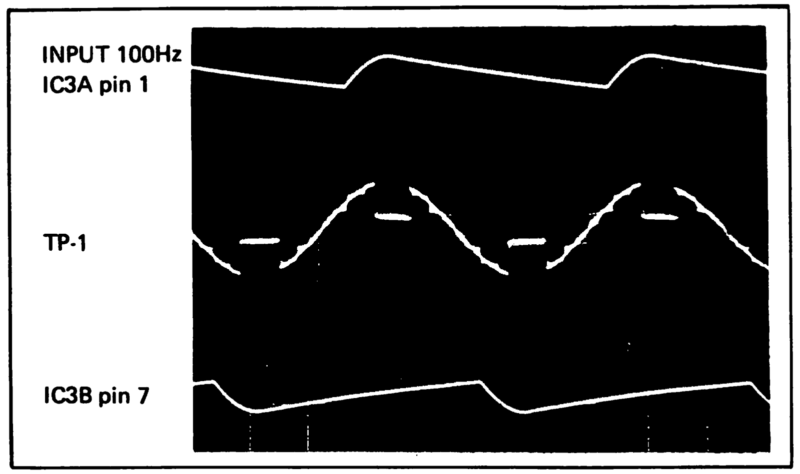
Fig. 2

The ideal companding system will work as follows:
With 100V, 10V and 1V input applied to the comparator (IC8) at different time, the D/A converter outputs the same successive voltages which are attenuated by IC10 by 1, 10 and 100 respectively before comparison. Consequently, the A/D converter has a higher resolution 100 times that of direct conversion at 1V input. The same procedure takes place, when RAM stored data are D/Aed as a delay signal, to correctly restore the voltage to the original level. Examples of companding effects are shown in the photos below.
Note that waveforms at TP-1 will change drastically as the input varies in level, especially at a border of ranges where companding system works even for one waveform cycle of low frequencies.
These phenomenons should be made familiar to the eye of observer to avoid misjudging.



PEAK HOLD & COMPARATOR (ICs 6 and 7)

The positive and negative peaks of a samped signal are peak-held and detected at IC6 and IC7 respectively, resulting in a logic code as shown in the table below. The code is latched into IC33 at SAH rate, passes through IC34 (data selector) on "L" DB5 (A/D cycle), and through ICs 35C and D and reaches pins 6 and 9 of IC10 D/A attenuator. IC10 switches ON or OFF its analog gates to provide for correct D/A output level.

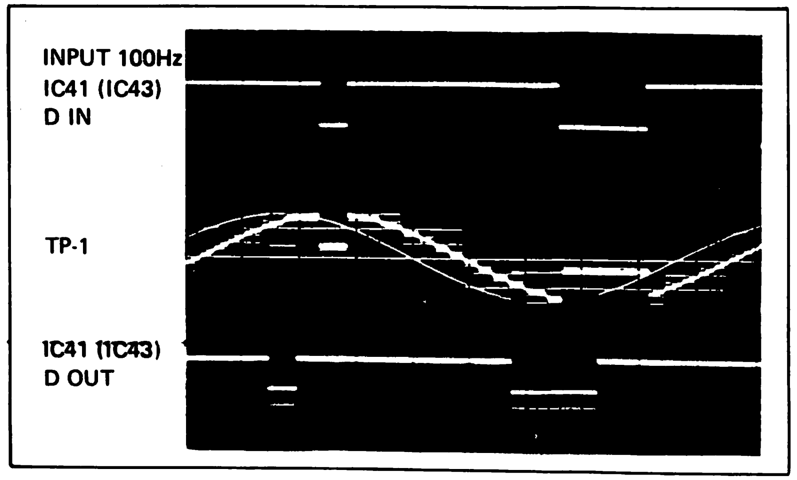


Vin	IC7 pins 7, 12	IC6 pins 7, 12	IC10 pin 6	IC10 pin 9
Vin ⟩ 1.99V	L	L	H	H
1.99V ⟩ Vin ⟩ 0.55V	L	H	H	L
0.55V ⟩ Vin ⟩ −0 55V	H	H	L	H
−0.55V ⟩ Vin ⟩ −1 99V	L	H	H	L
−1.99V ⟩ Vin	L	L	H	H

This logic code is also sent through IC33 to companding RAMs IC41 and IC43 while A/Ded input signal data is sent from comparator IC8 to RAM board via IC31. In other words, audio input is stored into two locations with different information separated—meter's pointer deflection reading into IC1—IC12 on the RAM board, and meter range into companding RAMs.

COMPANDING RAMs (IC41 and 43)

As shown in the Main Controller Timing Chart (see RAM1—RAM3) and RAM table, A/D data for a sampled signal is stored into three RAMs (in the same RS section) four times starting from MSB 3 bits (D11—D9).
On the contrary, companding data is stored into IC41 and IC43 once for the signal. However, since the same addresses are used for both RAM groups, companding RAMs cannot make use of the remaining three addresses if suitable modification is made on them. IC31 issues address-offset data from DB0 and DB1 to IC38 and IC36 (Address Adder) which adds 0 to 3 as the memory banks change from RS16 to RS32, RS32 to RS48 and so on.



When in delay mode (D/A cycle, IC31 DB5=H and DB6=L), companding data is latched into IC32 on rising edge of DB4, selected by IC34 (pin 1=H), gated by IC35C and D, then routed to IC10. With this companding data applied IC10 determines the range of analog voltage from D/A converter IC15 and IC14, restoring RAMs (IC1—IC12) stored data to the original signal level.

RAMs IC1—IC12 on RAM BOARD

As mentioned earlier, during successive approximation of a sampled signal, comparison results are stored into three RAMs, being designated by RS-, in 3 bits parallel x 4 serial format to represent the signal in 12 bit data. RAMs used for storing are always from those in RS16 (ICs 12, 8 and 4) to RS64 (ICs 9, 5 and 1) depending on delay time settings.
In short delay settings those RAMs of RS16 are repeatedly used while those in RS64 are left out of storing. This concept becomes important when troubleshooting RAMs. (Refer to the table on P.13).

CONTROL SIGNALS IN DIFFERENT MODES

SDE-3000	IC 30 P23	IC30 P14	x2 INDI-CATOR or IC 18 PIN 12	FOOT SW JAC: HOLD ON/OFF	FOOT SW JAC: DELAY ON/OFF	DELAY ON/OFF LED (D13)	IC 31 HOLD	A TR 24 GATE	B TR 25 GATE	C TR 41 GATE	D TR 53 GATE
Mute Operation	0	0	0	0	1	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0
	0	1	0	1	1	0	0	0	0	0	0
	0	1	0	1	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0
	0	1	1	1	1	0	0	0	0	0	0
	0	1	1	1	0	0	0	0	0	0	0
Noral Operation	1	0	0	0	1	0	0	0	1	0	0
	1	0	0	0	0	1	0	0	1	0	1
	1	1	0	1	1	0	1	0	0	0	0
	1	1	0	1	0	1	1	0	0	0	1
	1	0	1	0	1	0	0	1	0	0	0
	1	0	1	0	0	1	0	1	0	1	0
	1	1	1	1	1	0	1	0	0	0	0
	1	1	1	1	0	1	1	0	0	1	0
Remarks	0: 0V 1: 5V	0: 0V 1: 5V	0: 0V Indicator OFF 1: 5V Indicator ON	1: ON SW open 0: OFF SW closed or NOR-MAL	1: Cl SW closed 0: OF SW open or NOR-MAL	0: LED OFF 1: LED ON	0: 0V 1: 5V	0: −14V 1: 0V	0: −14V 1: 0V	0: −14V 1: 0V	0: −14V 1: 0V

* Irrelevant to Power-ON mute suc as MUTE A and MUTE B. All "0" during Power-ON MUTE periods.

DIAGNOZING DELAY SOUND

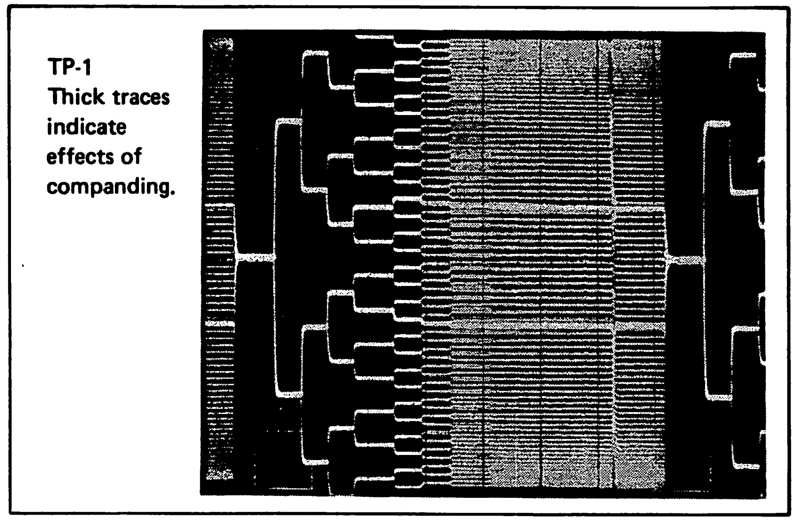
— Isolating Defective RAM —

▶For SDE-1000, see para. 5 and 6.
▶Also see P.22 for failure examples.

When a trouble is found in the delay sound, the circuits first to be checked will be those shown in the block diagram (Fig. 2, P.11).
They are closely related to each other. Of these, companding circuit effects to both A/D and D/A conversions and the D/A converter becomes a part of A/D converter during A/D cycle. However, the most difficult to point out is a RAM since 14 RAMs are involved in the delay line. Consequently, this section describes fault isolation procedure on the assumption that a specific RAM is defective.
Before going into RAM sections, other related circuits must be checked for proper function. These checkings also give hints for troubleshooting associated circuits.
NOTE: The number of RAM cells engaged in sound delay are dependent on delay time and the level of input signal while companding circuit acts with changes in input sound level. Unless otherwise directed DELAY TIME should be set at the longest and the input signal level varied widely when checking.
USE MONITOR for help checking irregular sound.

1. BRIEF CHECKING

With relatively large signal applied to the unit's input jack, observe TP-1 (IC14 pin 6); Adjust the scope to display the waveform similar to that in the photo below.
Check steps of A/D cycle traces for 1/2-changes in voltage. If not, widely vary the input level and check whether companding circuit is ill affecting.
When A/D conversion seems defective, proceed to para. 5.



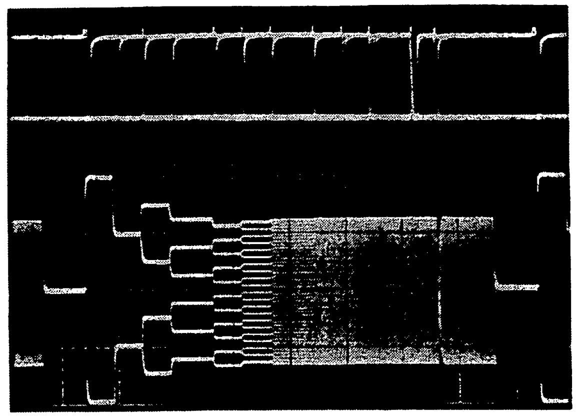
2. DISCONNECTING COMPANDING CIRCUIT

Companding circuit affects to both A/D and D/A converters. Disconnect the companding when checking the both circuits.

a. Disolder and remove the ground lead of R165 connecting to pin 6 of IC10.
b. Jumper wire across pin 6 of IC14 (TP-1) and pin 2 of IC8 to bypass IC10.

If companding circuit seems defective, proceed to the next para.

DIN of IC31
TP-1
Freed from companding effect.



3. COMPANDING CIRCUIT

When companding circuit seems malfunctioning, track the logic code from peak hold output to IC10 (see the table in "Peak Hold and Comparator" in the Circuit Description, SDE-3000). During a tracking the input signal must be set at a level for unchanged code. Then change input level for another logic code.
Verify the identical code throughout A/D and D/A cycles. If a difference exists, check RAMs IC41 and IC43.

4. ISOLATING RAM GROUPs (RS16—RS64)

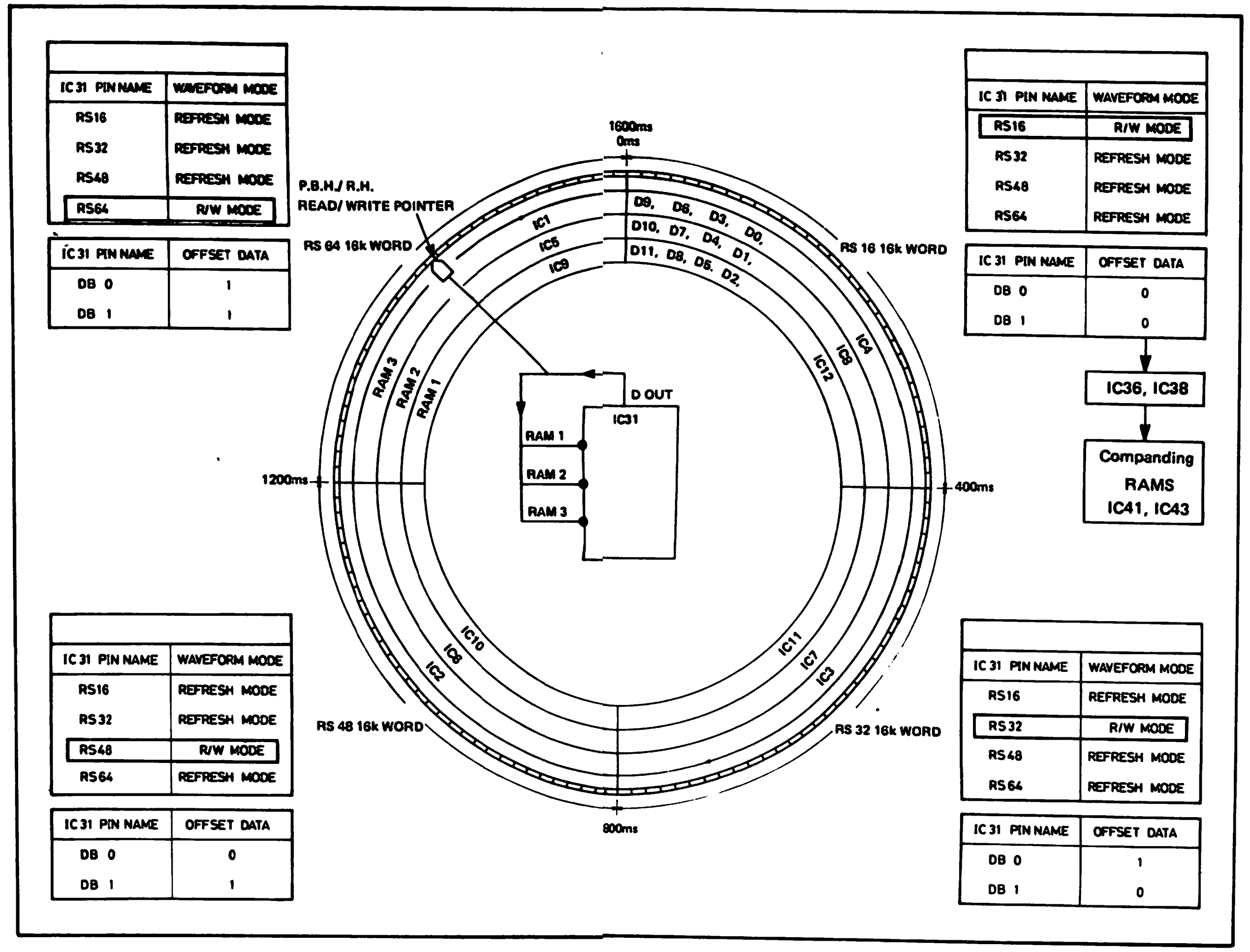
When delay time at which defective sound is reproduced is determined, it is easier to point out the RAM group containing the ill cell by referring to the table on the right.
The DELAY DISPLAY can be a great help to measure the time when abnormal sound occurs on the border of two RAM groups.

a. With MODULATION OFF, set TIME to the maximum.
b. Adjust DELAY TIME (X1-X1.5) on the rear panel for 1600ms display.
c. With MODULATION DEPTH "0", push MOD to ON.
d. Re-set TIME to around suspective time. For example, if a noise pops closely at the middle of the delay time, set TIME for 800ms. If the noise disappears, failure may be located anywhere in a RAM of RS48. Some errors may exist in relationship between the delay time and the RAM address increment (±1ms). In this critical case, refer to the next para.

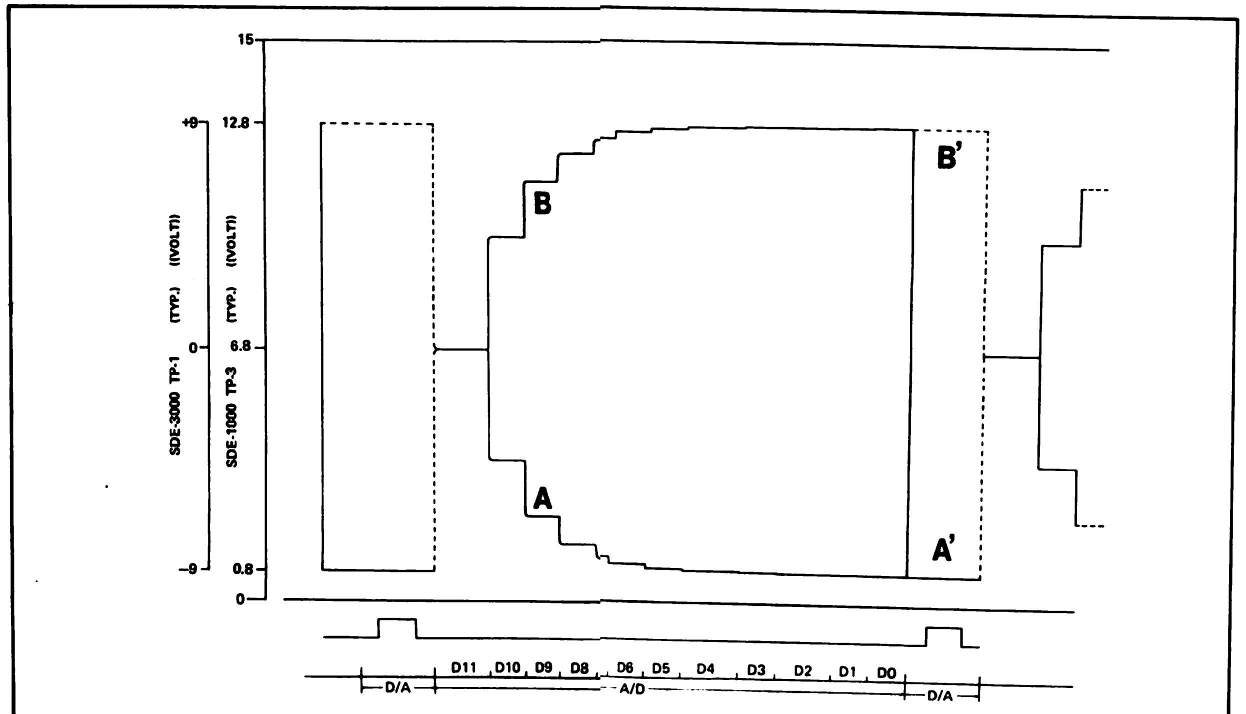
It is difficult to detect failure in lower bits, also proceed to the next para.

5. ALL "1" & ALL "0" CHECKs

Using sine wave as a test signal has adverse effects, that is, data in conversion system, RAM memory, etc. vary status from time to time as the input changes in level. When DC voltage at constant level is applied as an input signal, these data bits will stay at "1" or "0" at least for a certain period.



Ideally, this can be accomplished by applying DC voltages (of max. or min. that can be accomodated by A/D system) to the input of the comparator IC8. Alternative to this is pulling up or down of D IN (IC31 pin 31).
a. Disconnect D42 cathode from TR97 (circuit dia. F-22).
b. A staircase "A" as shown in the figure will be seen at TP-1.
c. Connect a length of wire to D42 anode (or DIN of IC31) and touch the other end of the wire to ground point. A reversed waveform "B" will appear.
D/A cycle is also inverted when the delay time comes; its amplitude being equal to that at the end of A/D cycle.



Checking A/D Cycle

A/D staircase must step by 1/2 in amplitude. If not, or uncertain because of lower bits, check suspective bit(s) on D11-D0 of IC31.

Checking D/A Cycle

The waveform (and sound) will be disturbed at the moment when defective bit is reproduced. Check for jitter or glitch (pulse) at TP-1. If doubtful, proceed to para 6.

6. PINPOINTING DEFECTIVE RAM

Set DELAY TIME for 1600ms (see para. 4).
Feed D IN of IC31 with +5V or 0V (para. 5).
Connect scope to the bus of RAMs including suspective RAM. If the RAM is not defined yet, may have to be repeated for the other 2 buses.
For confirmation, first disconnect suspective RAM's D OUT by cutting off the pattern to the bus, then observe the RAM D OUT directly.

SDE-1000 ENGINEERING CHANGE

Earier SDE-1000's have factory-modifications on INPUT Switch, Head Amp, Expander and Compressor as shown in the table below. The modifications add the following features (one by one) to the unit when it is used with UNI-GAIN set in –20dBm.

* Greater Delay circuit headroom with better balance of Direct/Delay sounds in volume.
* Higher frequency response of the Delay line.
* Greater S/N ratio in Delay sound.

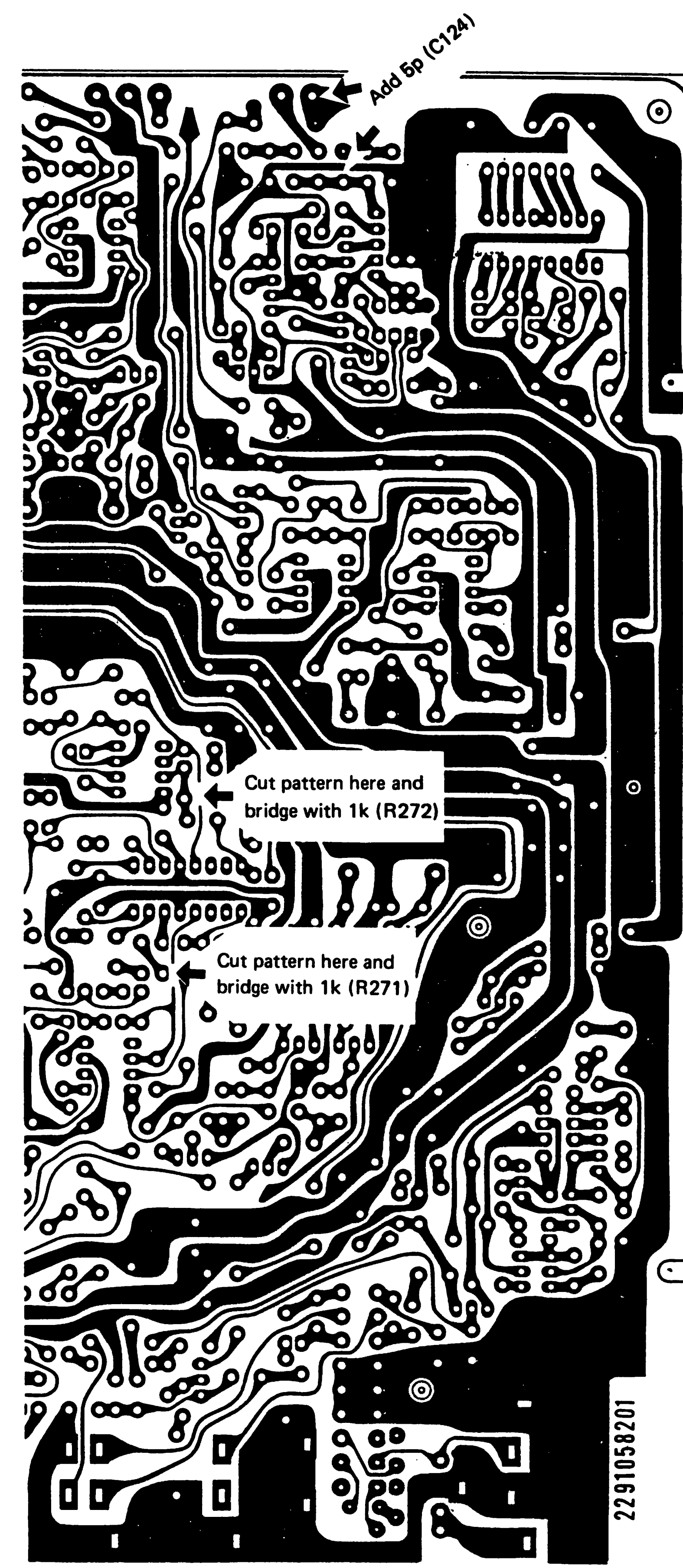
When need arises to implement one of the aboves to a given unit with serial number prior to 374800, the final values in the bottom of list should be applied since these improvements closely relate to each other.
Exceptions are R271 and R272 whichcan be solely implemented for reducing noise from compander.

NOTE: Changed parts are mounted in place on the parts side of the PCBs of 2291058202 and subsequent versions.

SERIAL No.	PCB Version	R39 Ω	R40 Ω	R42 Ω	R45 Ω	R108 Ω	R145 Ω	R260 Ω	R271 & R272 Ω	R58 Ω	R61 Ω	R189 Ω	R224 Ω	C114 F	C124 F	C48 F	MAX. INPUT LEVEL before clipping: DIRECT	MAX. INPUT LEVEL before clipping: DELAY	INPUT –20dBm
320100–320699	2291058200	56K	18K	560	6.8K	56K	180K	3.3K	0Ω	15K	33K	47K	0Ω	47P	22P	0P	IN ATT: 0dBm UNIGAIN: –20dBm		
330700–342149													680	100P	0P				LO 56KΩ
352150–353099	2291058201															5P	–8dBm	–8dBm	
363100–364799		∞		1K				5.6K		8.2K	12K	27K			5P See right		–3dBm	–8dBm	HIGH 560KΩ
374800–			10K		3.9K	68K	220K		1K See right	15K	33K	47K					–3dBm	–3dBm	HIGH 560KΩ
	2291058202	∞	10K	1K	3.9K	68K	220K	5.6K	1K	15K	33K	47K	680	100P	5P	5P			

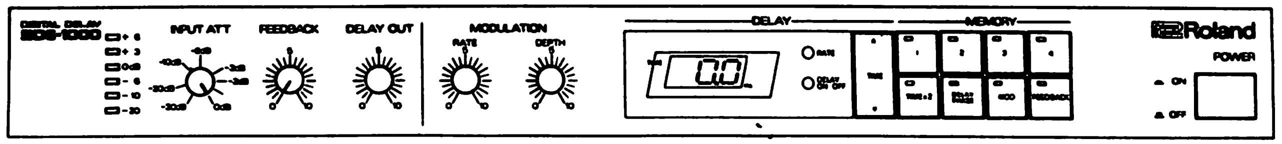
LOCATIONS

R39, R42(SW1A) R45(SW1B)/R108(IC8)/R224, C114(Q55)
C124(VR6–SW1A) R40(SW1C)/R145, R272(IC15 pin 5)/
R271(IC15 pin 12)
C48(Q13–Q18) R189(IC30 pin 2)/R260(Q57)/R58, R61(Q18–JK3)



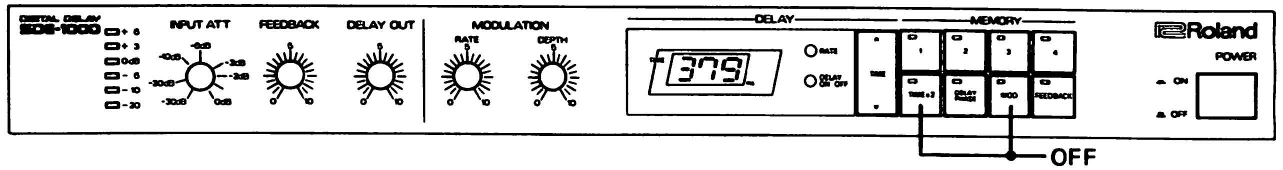
SDE-1000 ADJUSTMENT

1. LEVEL METER CALIBRATION



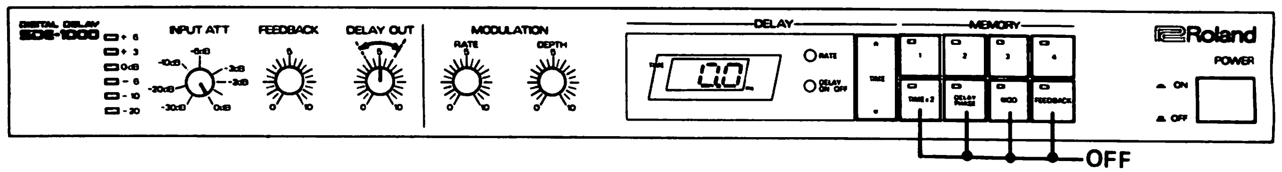
1-1. Set UNIGAIN (Rear panel) to –20dBm.
1-2. Connect audio generator (AG) to INPUT jack and set AG for –20dBm, 1kHz, sine.
1-3. Set RT8 at the point where +3dB LED just completely fades out.

2. DELAY TIME



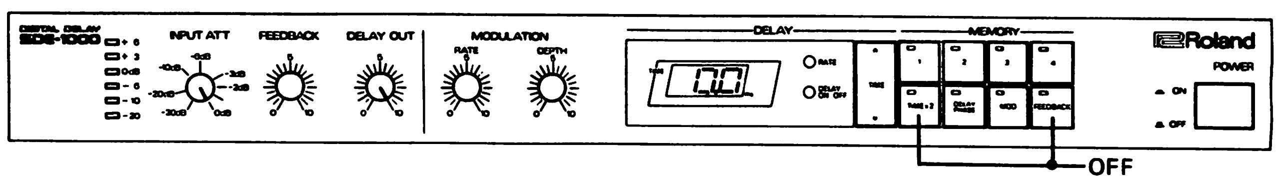
2-1. Set DELAY TIME (VR1, Rear panel) to X1.
2-2. Press and hold DELAY TIME button until DELAY TIME display reads maximum value.
2-3. Adjust RT6 for 379 ± 1ms reading.
2-4. Repeat step 2-2. If the reading changes, readjust RT6 for 379 ± 1ms.

3. COMPRESSOR LEVEL LINEARITY

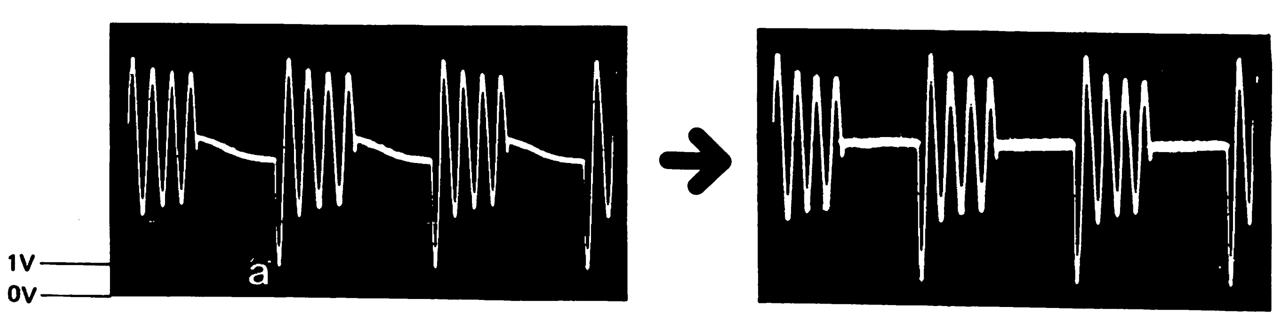


3-1. Set DELAY TIME (Rear panel) to X1 and UNIGAIN to –20dBm.
3-2. Connect AG to INPUT jack and set for –10dBm, 1kHz, sine.
3-3. Adjust DELAY OUT (VR4) for –10dBm reading.
3-4. Reset AG to –60dBm. Adjust RT1 for –60 ± 0.5dBm reading.
3-5. VR4 and RT1 interact. Repeat from 3-2 through 3-4.

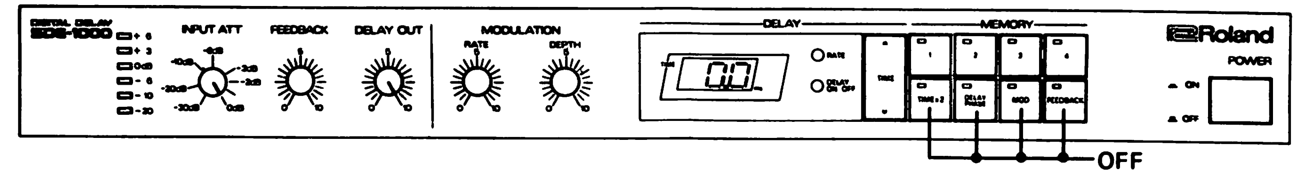
4. COMPRESSOR TOTAL HARMONIC DISTORTION



TEST POINT: TP2 (connect to oscilloscope - - DC coupling)
4-1. Set DELAY TIME to X1 and UNIGAIN to –20 dBm.
4-2. Connect AG to INPUT jack and set for 1kHz, sine, burst tone (4-0-4 cycles). Adjust AG output level so that the first bottoms (a) are at +1V on the scope.
4-3. Adjust RT2 for straight DC level.
4-4. Set scope V IN to AC coupling.
4-5. Repeatedly rotating INPUT ATT over its full travel, fine adjust RT2 for minimum DC drift.
Adjust scope VAR as necessary.

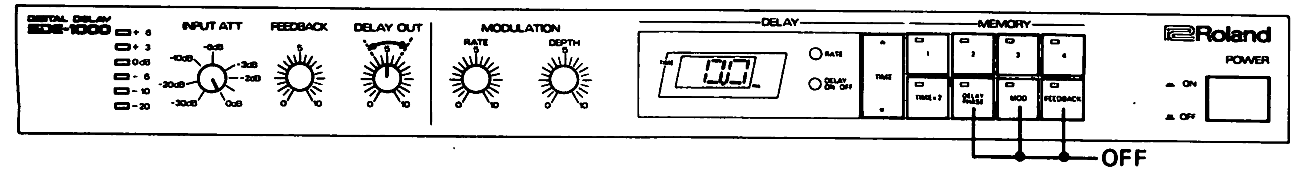


5. EXPANDER TOTAL HARMONIC DISTORTION



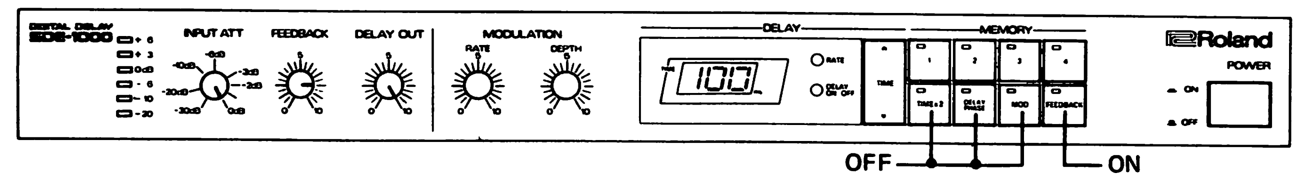
TEST POINT: DELAY OUT (connect to scope - - DC coupling)
5-1. Set DELAY TIME to X1 and UNIGAIN to –20dBm.
5-2. Feed the same signal as for 4-2.
5-3. Adjust RT3 for straight DC line.
5-4. Set scope V IN to AC coupling.
5-5. Repeatedly rotating INPUT ATT over its full travel, fine adjust RT3 for minimum DC drift.
Adjust scope VAR as necessary.
5-6. Connect amplifier/speaker to DELAY OUT and check for pop or rumble noise. If noticeable, check for absence of R271 and R272 (see table on the facing page) which are effective to the problem.

6. FREQUENCY RESPONSE



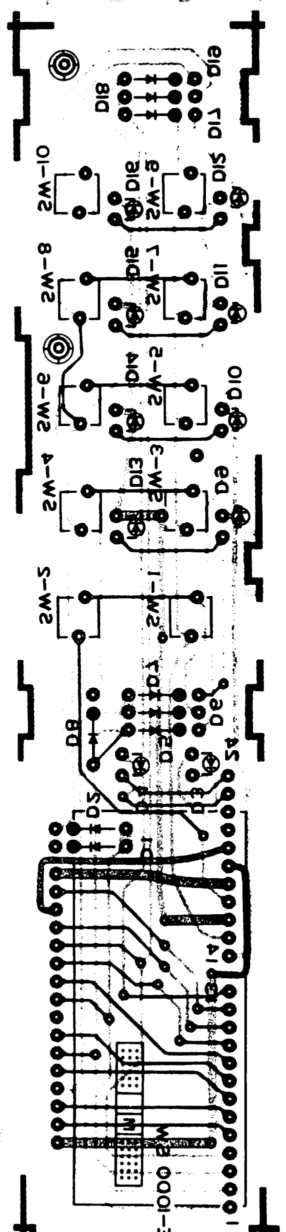
TEST POINT: DELAY OUT (connect to AC voltmeter)
6-1. Set DELAY TIME to X1 and UNIGAIN to –20 dBm.
6-2. Connect AG to INPUT jack and set AG output for –20dBm, 1kHz, sine.
6-3. Adjust INPUT ATT for –30dBm reading.
6-4. Reset AG to 8.5kHz.
Adjust RT4 for –30.2dBm reading.
6-5. Press DELAY TIME X2 (ON). Reset AG to 400Hz, –30dBm.
6-6. Adjust INPUT ATT for –30dBm reading.
6-7. Reset AG to 5kHz, –30dBm.
Adjust VR5 for –30.2dBm reading.

7. FEEDBACK



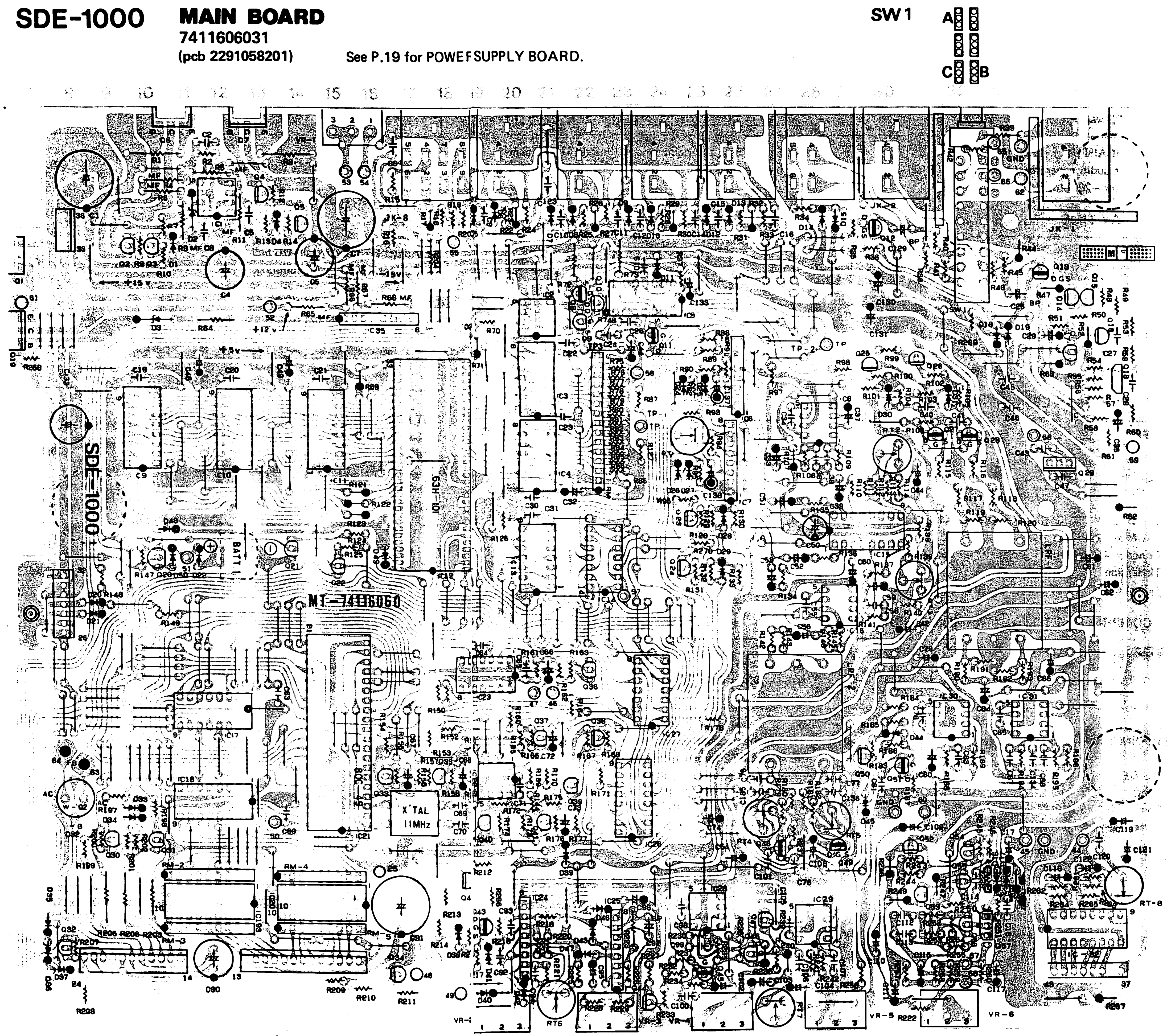
TEST POINT: DELAY OUT (connect to scope)
7-1. Set DELAY TIME to X1 and UNIGAIN to –20 dBm.
7-2. Apply a signal (e.g. –30dBm, 1kHz, sine) to INPUT jack for an instant and adjust RT7 for continual repeats at a level.
7-3. Verify decaying repeats with FEEDBACK at 7.5.

SWITCH BOARD
7411608005
(pcb 2291058400)
View from foil side

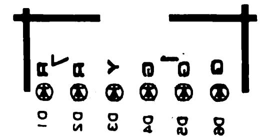


SDE-1000 MAIN BOARD
7411606031
(pcb 2291058201)

See P.19 for POWEFSUPPLY BOARD.

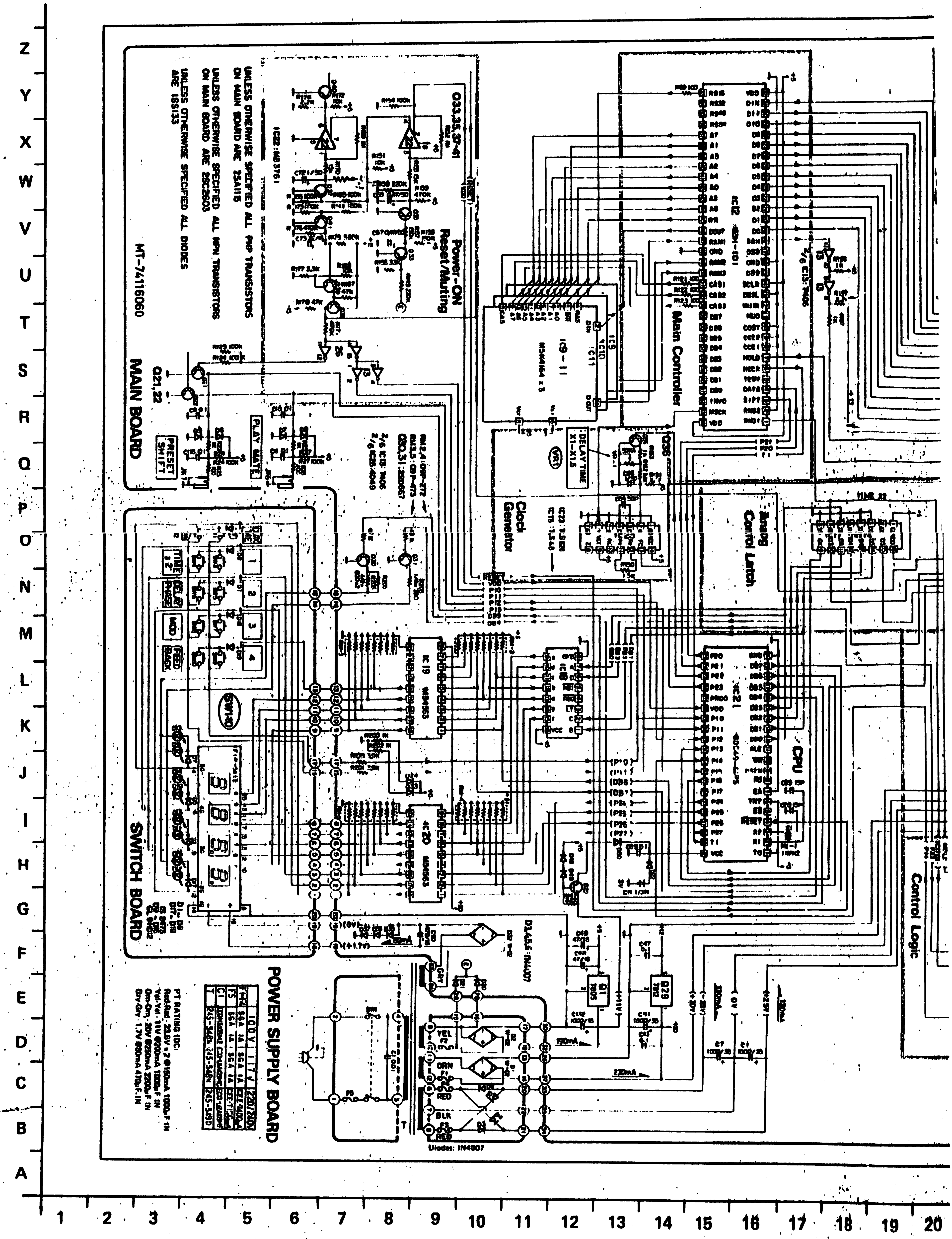


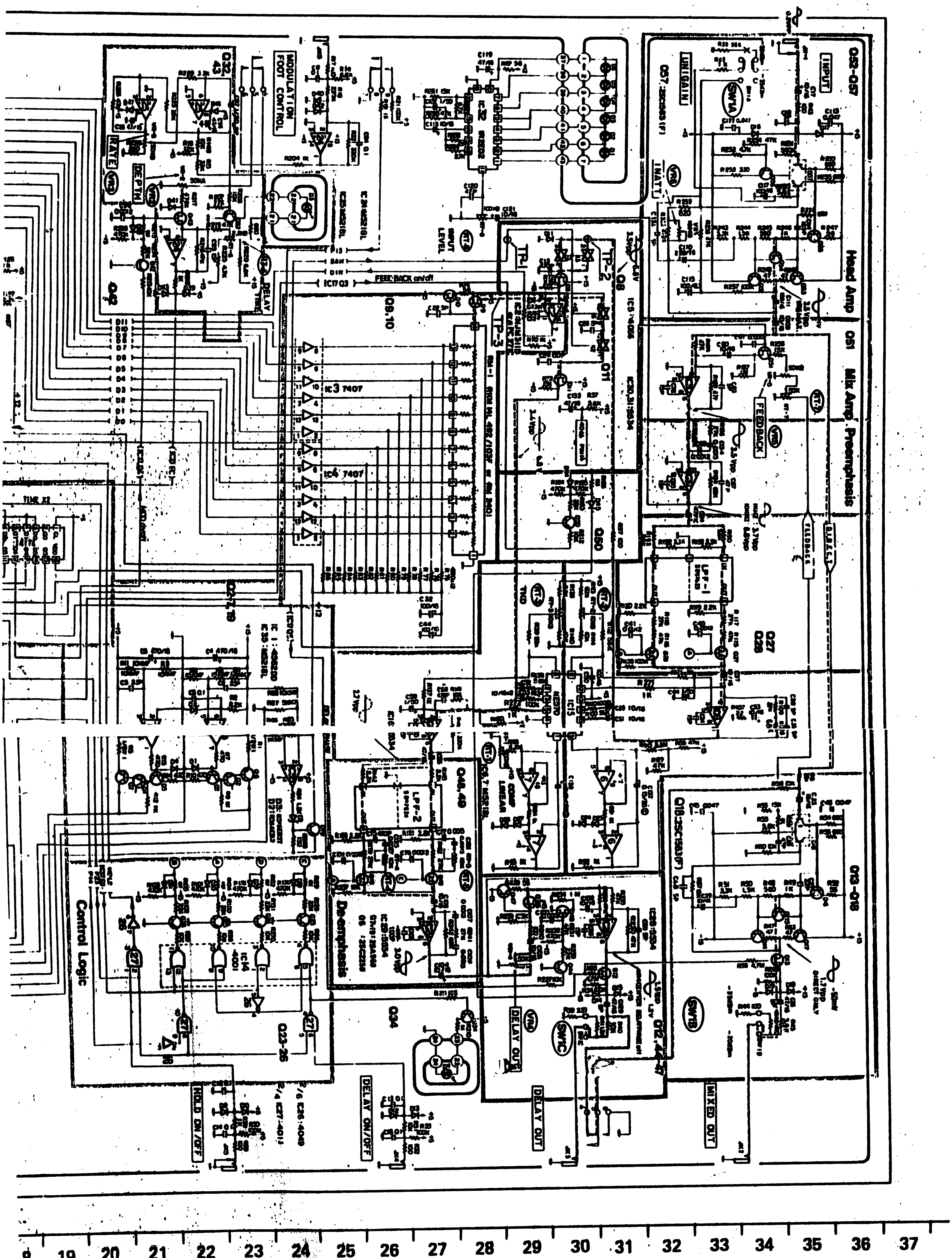
LED BOARD
7411607001
(pcb 2291058300)
View from foil side



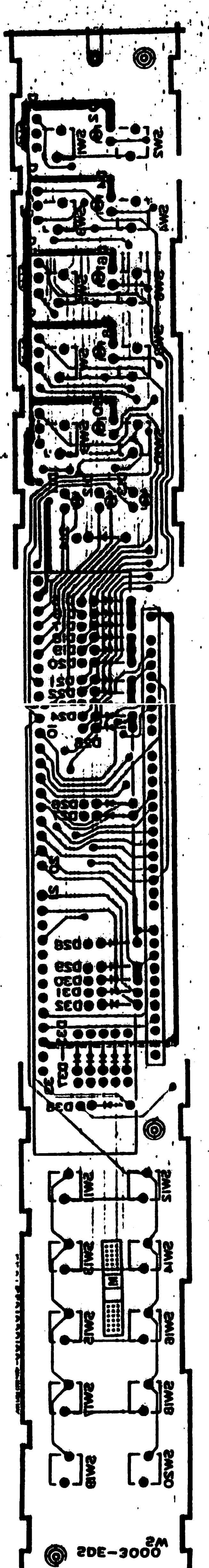
FEB. 5, 1984

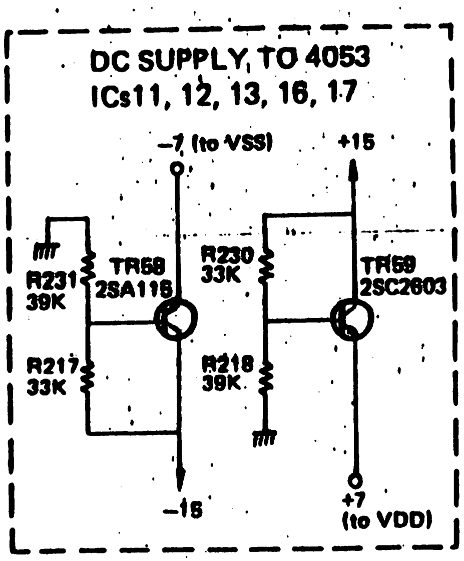
SDE-1000 CIRCUIT DIAGRAM

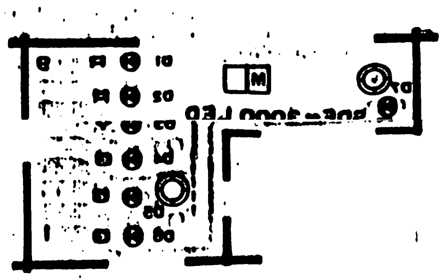



Head Amp
Mix Amp, Preemphasis
Control Logic
De-emphasis
MODULATION FOOT CONTROL
INPUT
UNITY GAIN
FEEDBACK
DELAY OUT
MIXED OUT
HOLD ON/OFF
DELAY ON/OFF
RATE
DEPTH
IC3 7407
IC4 7407
TIME X2
TP-1
TP-2
TP-3
8
19
20
21
22
23
24
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26
27
28
29
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32
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SDE-3000
CIRCUIT DIAGRAM

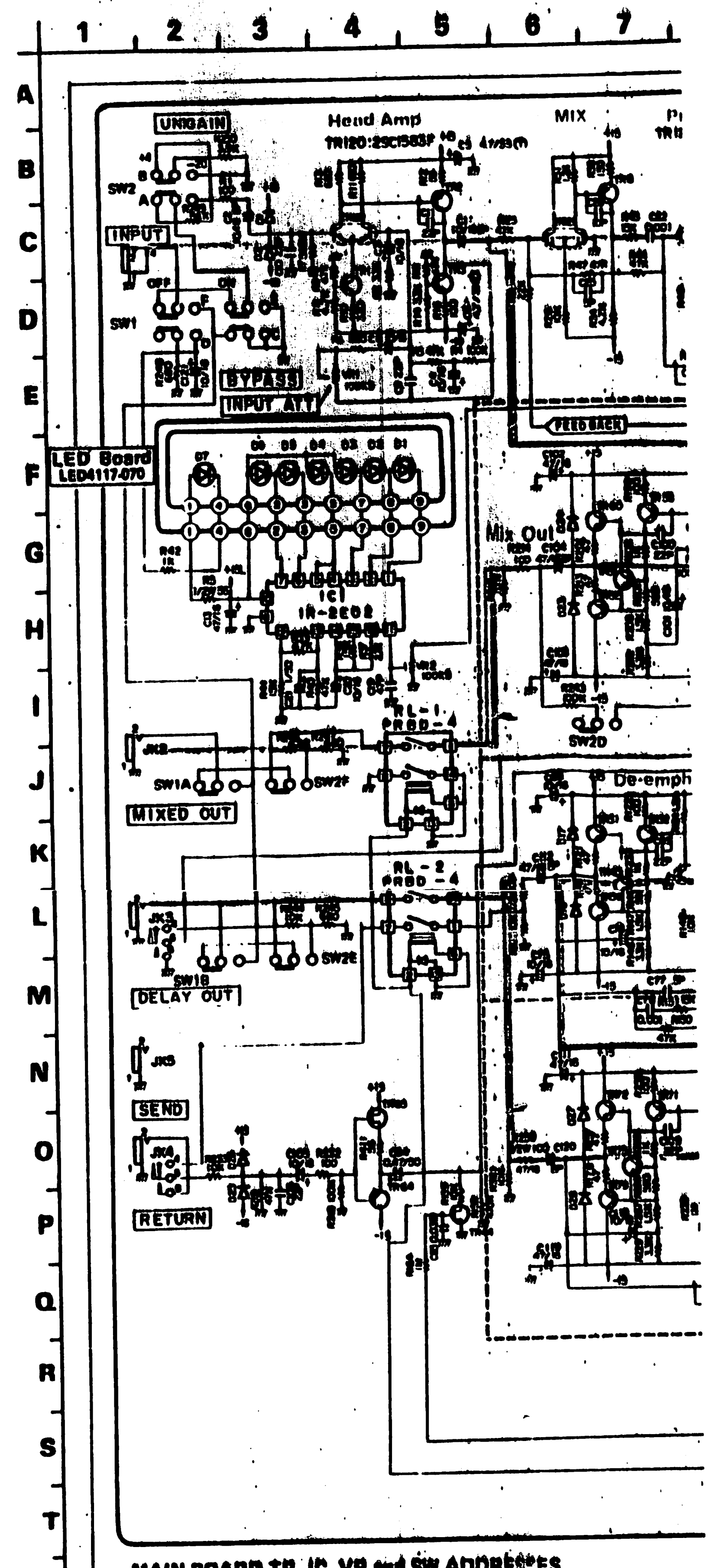






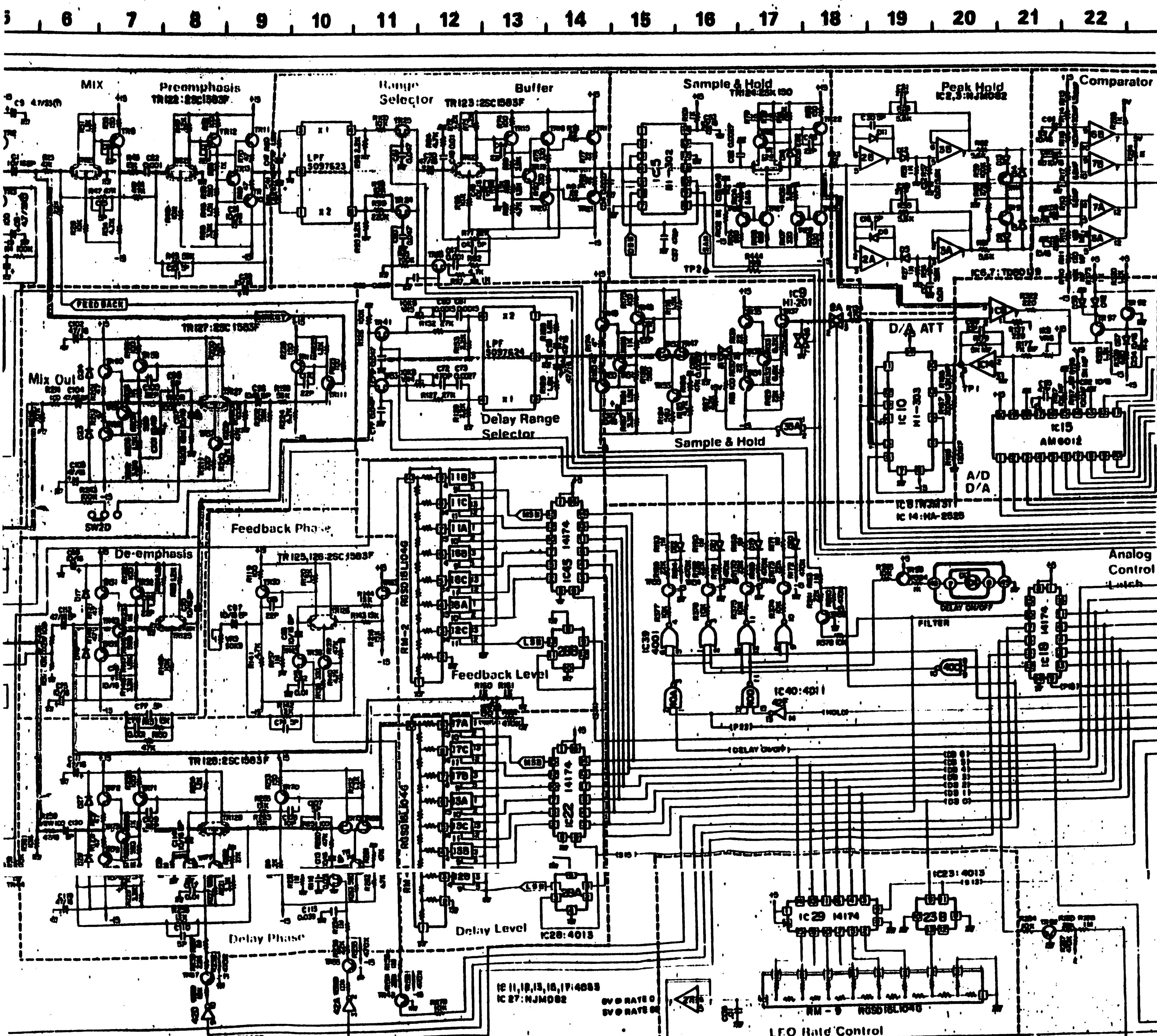
LED BOARD
7411707001
(pcb 2291058000)
View from foil side

SWITCH BOARD
7411708005
(pcb 2291058100)
View from foil side

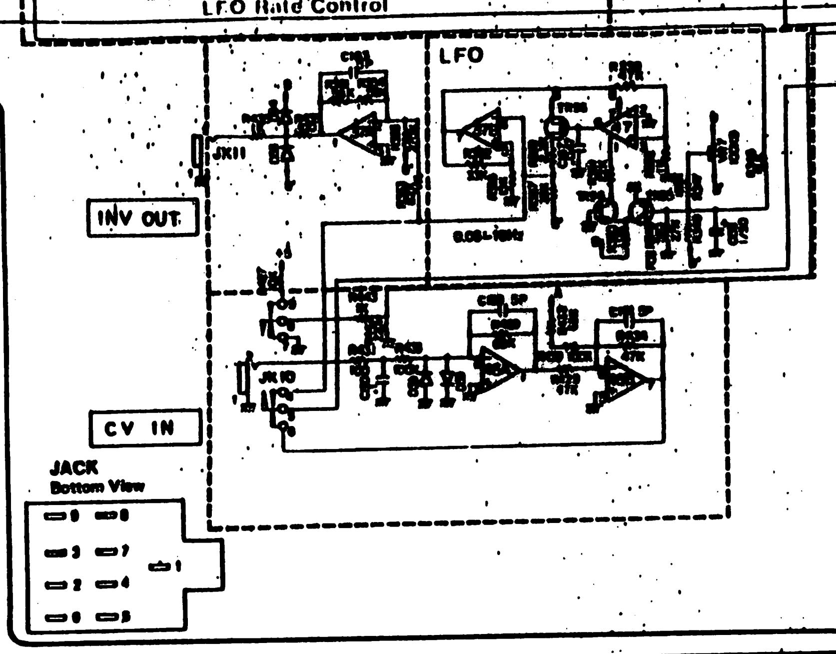


MAIN BOARD TR, IC, VR and SW ADDRESSES

TR										
1	:D-4	27	:D-17	53	:G-15	79	:P-7	105	:L-41	1
2	:C-5	28	:D-17	54	:K-16	80	:D-36	106	:O-41	2A
3	:D-5	29	:D-18	55	:K-15	81	:E-36	107	:P-39	2B
4	:Y-35	30	:K-9	56	:G-7	82	:O-3?	108	:O-41	3A
5	:Y-35	31	:K-7	57	:H-8	83	:W-29	109	:O-42	3B
6	:W-35	32	:K-7	58	in separate	84	:W-28	110	:U-31	4
7	:X-35	33	:G-11	59	figure	85	:X-27	111	:G-10	4
8	:B-7	34	:G-17	60	:G-7	86	:X-27	112	:G-10	5
9	:D-21	35	:F-17	61	:H-7	87	:O-3?	113	:Y-36	6A
10	:D-9	36	:G-17	62	:H-7	88	:Y-27	114	:W-35	6B
11	:B-9	37	:F-17	63	:K 11	89	:X-28	115	:V-33	7A
12	:B-8	38	:L-10	64	:P-4	90	:U-28	116	:L-39	7B
13	:C-9	39	:L-7	65	:O-4	91	:U-28	117	:M-39	8
14	:C-21	40	:L-7	66	:R-10	92	:P-3?	118	:O-37	8A
15	:B-13	41	:F-11	67	:R-8	93	:U-2?	119	:not used	9B
16	:B-14	42	:G-11	68	:K-16	94	:V-21	120	:C-4	9C
17	:B-14	43	:L-10	69	:O-11	95	:V-21	121	:C-6	9D
18	:B-17	44	:P-8	70	:O-9	96	:U-20	122	:C-8	10
19	:C-13	45	:F-14	71	:O-7	97	:P-22	123	:C-12	11A
20	:D-13	46	:F-15	72	:O-7	98	:K-19	124	:C-17	11B
21	:D-14	47	:F-18	73	:O-10	99	:O-24	125	:L-8	11C
22	:B-18	48	:K-17	74	:P-10	100	:R-38	126	:K-10	12A
23	:E-12	49	:K-17	75	:O-7	101	:R-38	127	:G-8	12B
24	:D-11	50	:G-14	76	:P-10	102	:R-30	128	:O-8	12C
25	:B-11	51	:G-15	77	:P-8	103	:P-40			13A
26	:D-17	52	:F-15	78	:P-8	104	:M-41			13B



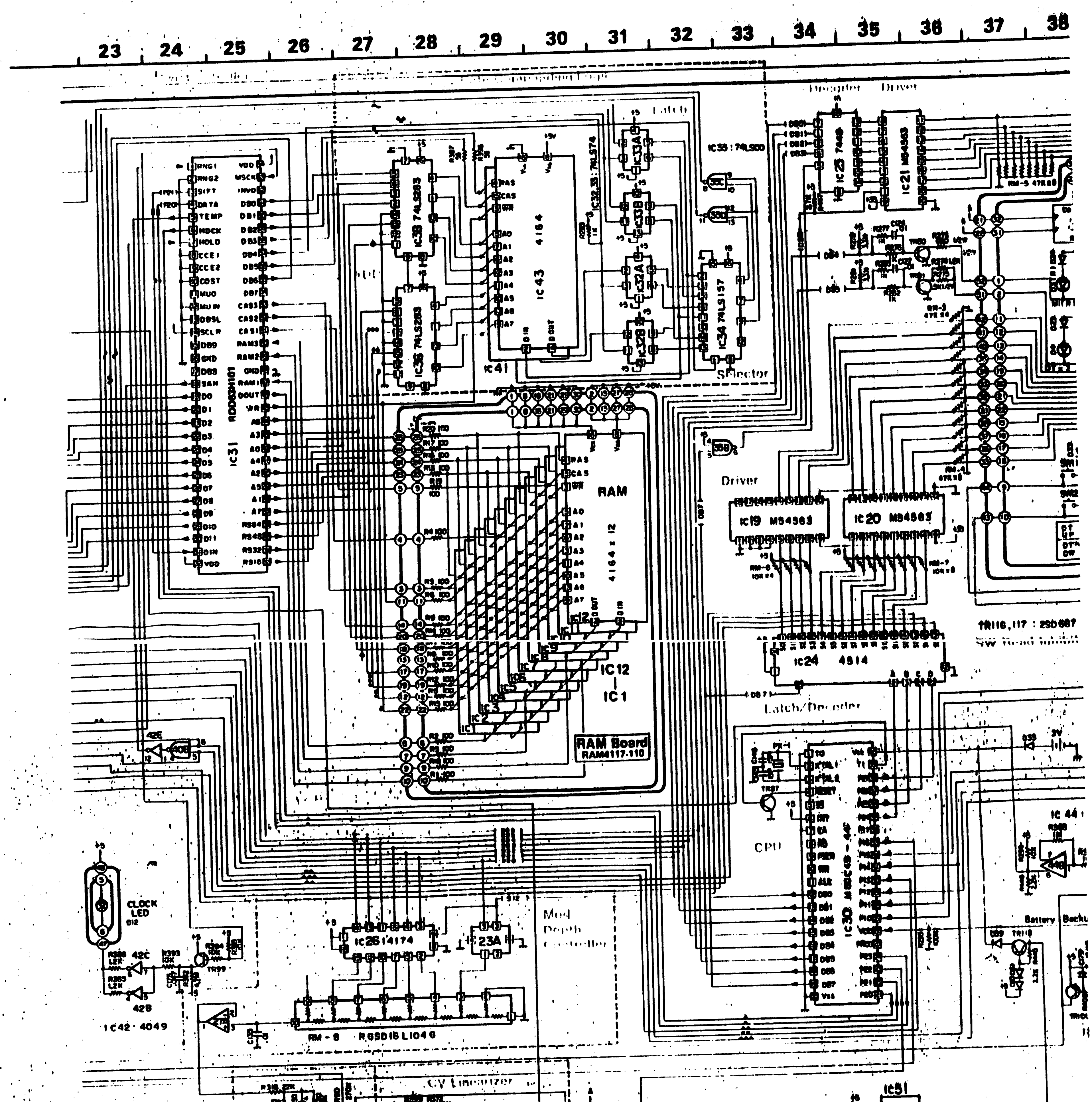
Main Board MT4117-080



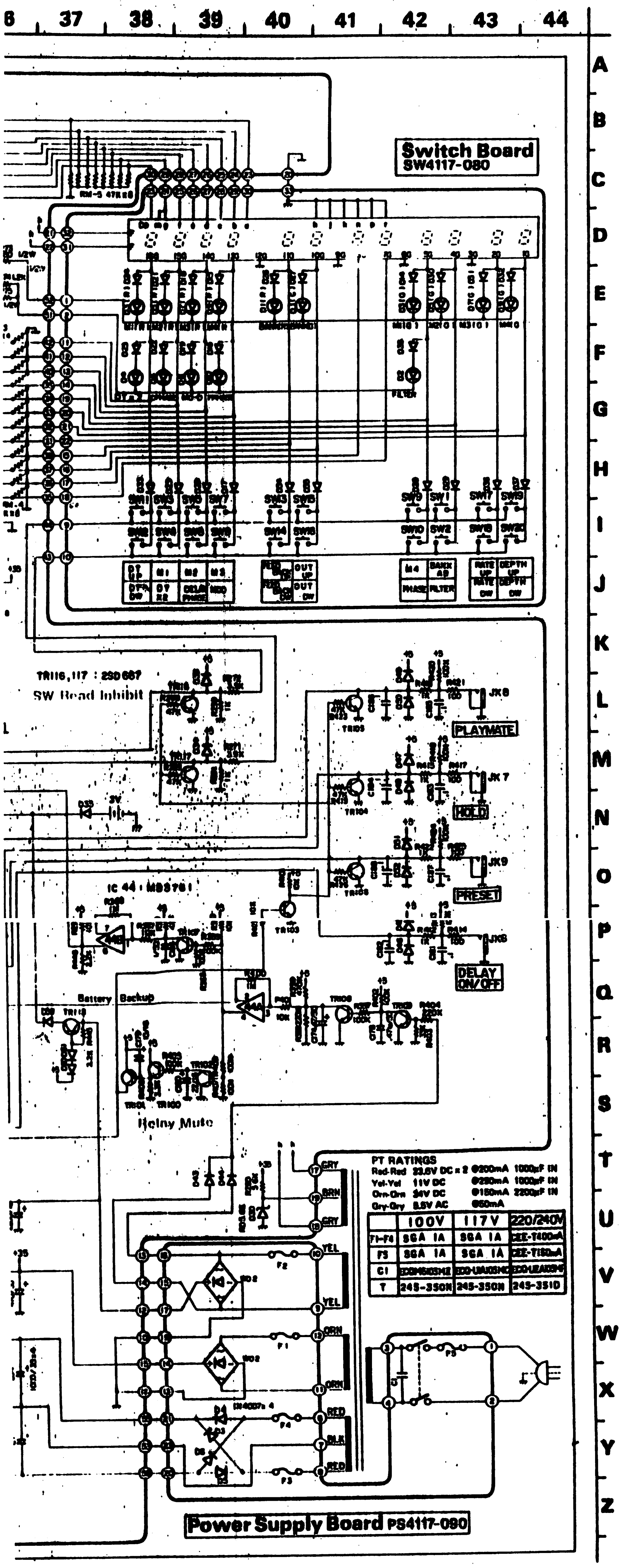
'DRESSES

		IC				VR
9 : P-7	105 : L-41	1 : H-4	13C : O-12	32A : E-31	44A : O-40	1 : E-4
0 : D-36	106 : O-41	2A : E-18	14 : O-20	32B : F-31	44B : P-38	2 : I-6
1 : E-36	107 : P-39	2B : C-18	15 : H-21	33A : B-31	45 : J-14	3 : L-9
2 : O-3?	108 : O-41	3A : E-20	16A : K-12	33B : D-31	46A : W-20	4 : G-1
3 : W-29	109 : O-42	3B : C-20	16B : J-12	34 : F-32	46B : X-21	5 : F-11
4 : W-28	110 : U-31	4 : X-34	16C : K-12	35A : H-17	47 : U-21	6 : F-21
5 : X-27	111 : G-10	4 : Y-34	17A : M-12	35B : H-32	48 : U-26	7 : U-22
6 : X-27	112 : G-10	5 : C-18	17B : N-12	35C : C-32	49A : U-28	8 : U-30
7 : O-3?	113 : Y-35	6A : E-22	17C : N-12	35D : D-32	49B : U-27	**SW**
8 : Y-27	114 : W-35	6B : E-22	18 : L-21	36 : F-28	50A : W-24	SW1A : J-2
9 : X-26	115 : V-35	7A : D-22	19 : I-33	37A : U-18	50B : X-29	SW1B : M-2
0 : U-28	116 : L-39	7B : C-22	20 : I-35	37B : U-19	51 : T-35	SW1C,E : D-3
1 : U-28	117 : M-39	8 : F-21	21 : C-36	38 : D-28		SW1D,F : D-2
2 : P-3?	118 : O-37	9A : F-18	22 : N-14	39 : L-15		SW2A,B : B-2
3 : U-2?	119 : not used	9B : F-17	23A : O-29	40A : M-15		SW2C : UNUSED GROUNDED
4 : V-21	120 : C-4	9C : not used	23B : O-19	40B : M-24		
5 : V-21	121 : C-6	9D : F-18	24 : L-34	40C : L-20		SW2D : I-7
6 : U-20	122 : C-6	10 : H-19	25 : C-35	40D : M-17		SW2E : M-3
7 : F-22	123 : C-12	11A : J-12	26 : O-27	41 : F-29		SW2F : J-3
8 : K-19	124 : C-17	11B : I-12	27A : S-24	42A : S-10		
9 : O-24	125 : L-6	11C : I-12	27B : S-16	42B : R-23		
00 : R-36	126 : K-10	12A : not used	28A : P-14	42C : Q-23		
01 : R-38	127 : G-6	12B : P-12	28B : L-14	42D : S-8		
02 : R-35	128 : O-6	12C : L-12	29 : O-18	42E : M-24		
03 : P-40		13A : O-12	30 : O-34	42F : M-17		
04 : M-41		13B : P-12	31 : H-25	43 : E-30		

FEB. 5, 1984

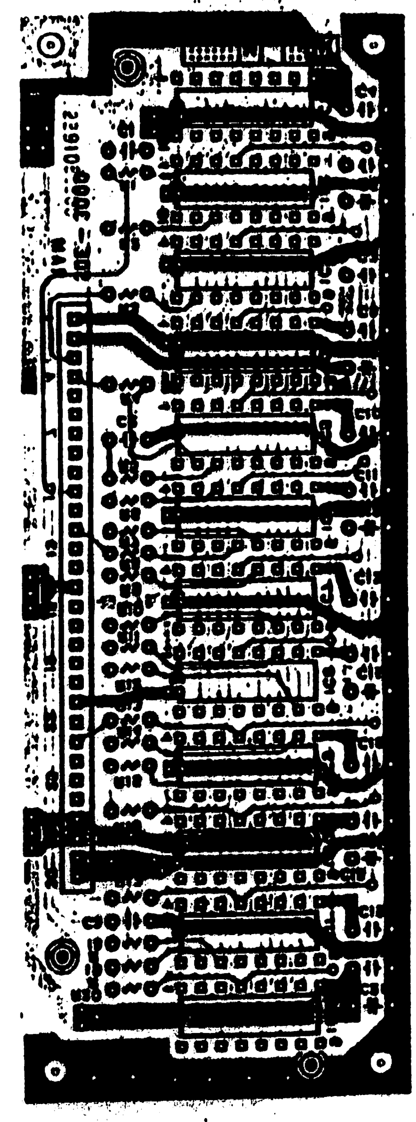


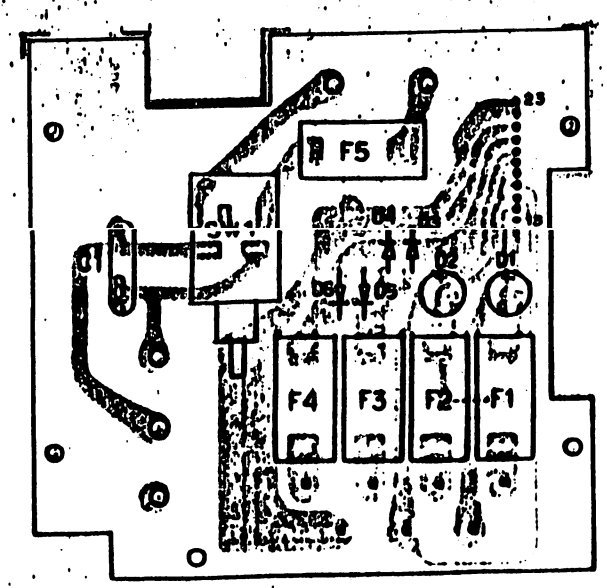
23
24
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29
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31
32
33
34
35
36
37
38
Latch
Decoder
Driver
IC35 : 74LS00
IC25 7448
IC21 M54563
IC38 74LS283
IC36 74LS283
IC43
4164
IC41
IC32,33 : 74LS74
IC33A
IC33B
IC32A
IC32B
IC34 74LS157
Selector
IC31
RAM
4164 x 12
IC12
IC1
RAM Board
RAM4117-110
Driver
IC19 M54563
IC20 M54563
IC24 4514
Latch/Decoder
TR116,117 : 2SD687
CPU
IC30
IC44
Battery Backup
CLOCK LED
IC42 : 4049
IC26 14174
23A
Mod Depth Controller
RM-8 RGSD16L104G
CV Linearizer
Mod depth
AGC
IC51
7805
S5500G
2SC2238
IC4 : 4562
2SA968
IC37 : 082
IC46,49,50 : M5216L
IC47,48 : BA662
TR85,86 : 2SC1923R
Unless otherwise specified all NPN transistors on main board are 2SC2603
Unless otherwise specified all PNP transistors on main board are 2SA1115



RAM BOARD

7411711002
(pcb 2291083800)
View from foil side





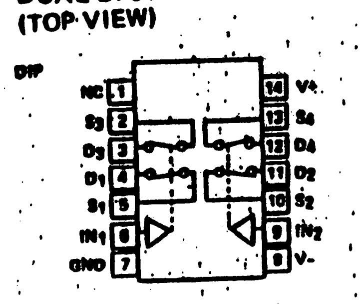
POWER SUPPLY BOARD

7411709000
(pcb 2291058500)

Common to SDE-1000 and SDE-3000 Fuses, Fuse labels. Capacitor C1 excluded. Specify model and line voltage when ordering for complete assy.

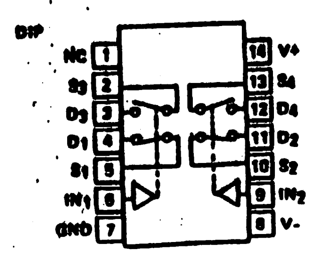
SDE-1000/SDE-3000共通

DUAL DPST HI-302 & HI-306
(TOP VIEW)



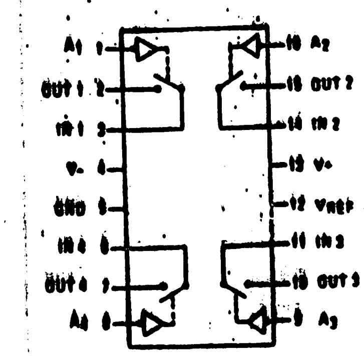
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

HI-201
(TOP VIEW)



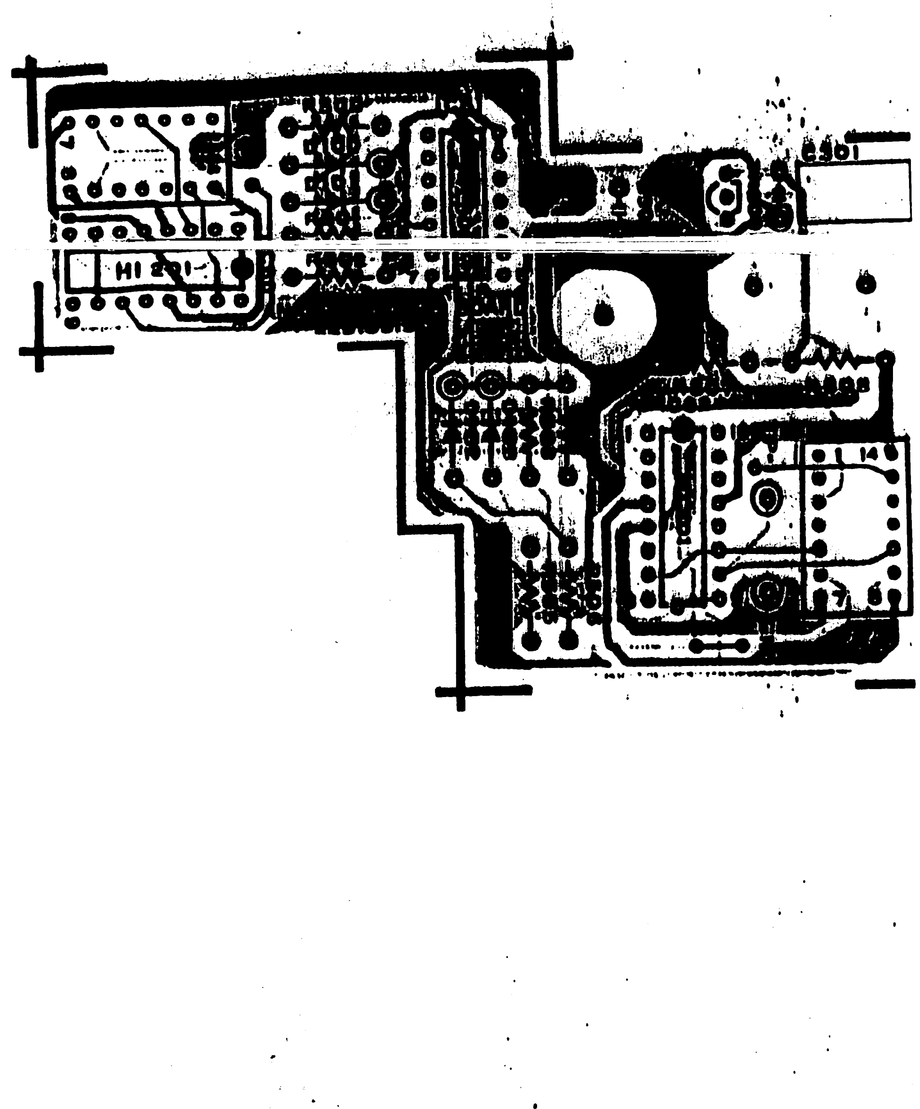
ANALOG SWITCH BOARD 2291091900

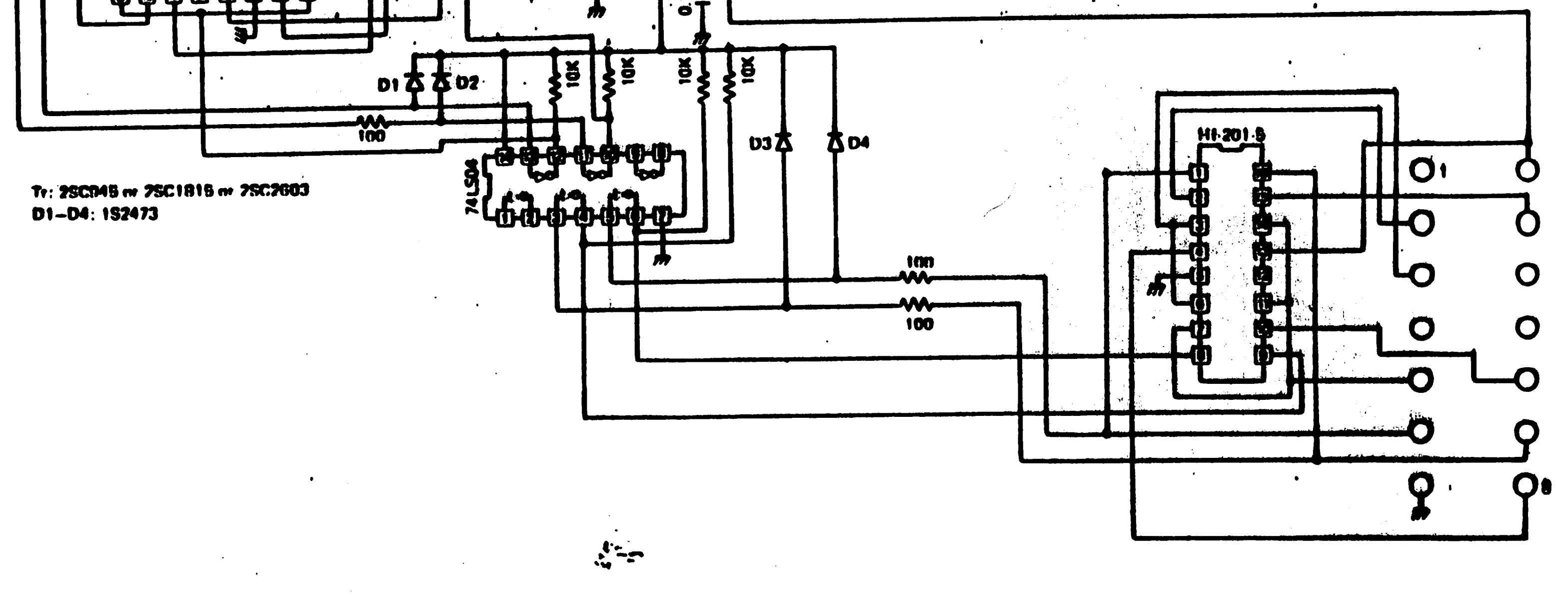
Temporarily used for SN 372900–395099

– Substitutive for IC5 HI-302 and IC10 HI-303 –

Analog Switch Board 2291091900 is equivalent to HI-303 and HI-302 in operation and is installed on some units because of ICs procural problem. When the PCB needs replacing, use regular ICs for IC5 and IC10 respectively.

一部の製品にはIC5 HI-302及びIC10 HI-303のかわりに、HI-201を使用した本基板(回路は全く等価)が取り付けられています。従って、上記2種類のICを使用した場合、本基板は不要となります。

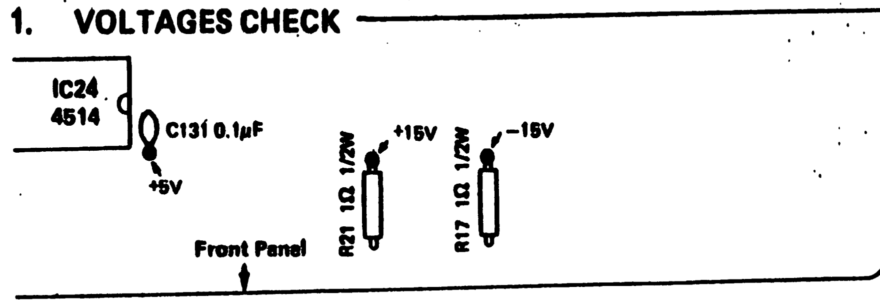




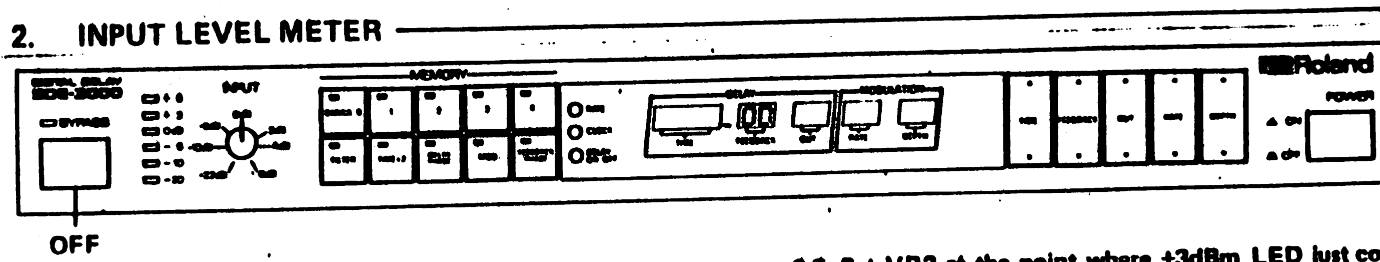
Tr: 2SC945 or 2SC1815 or 2SC2603
D1–D4: 1S2473

SDE-3000 ADJUSTMENT

1. VOLTAGES CHECK



2. INPUT LEVEL METER



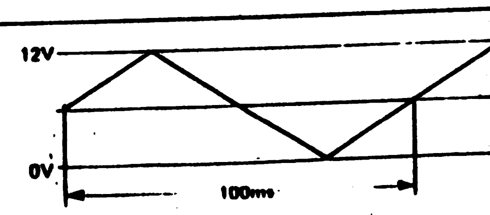
2-1. Set UNIGAIN (Rear panel) to +4dBm.
2-2. Connect audio generator (AG) to INPUT jack and set AG output for +4dBm, 1kHz, sine.
2-3. Set VR2 at the point where +3dBm LED just completely fades out.

3. VCO

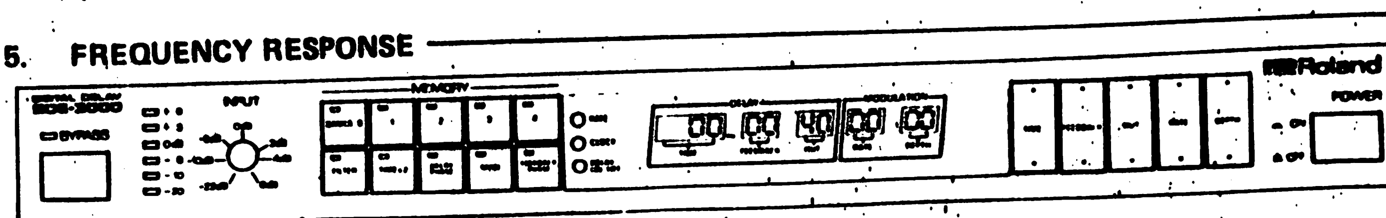
3-1. Set DELAY TIME (Rear panel) to X1.
3-2. Press and hold DELAY TIME button until TIME display reads maximum value.
3-3. Press TIME X2 (ON).
3-4. Adjust L1 for 3010±1ms reading.
NOTE: A TIME display change delays 1sec behind a coil adjustment.

4. LFO RATE

TEST POINT: MODULATION CV INV OUT (connect to oscilloscope)
4-1. Press and hold RATE button until RATE display reads 99.
4-2. Adjust VR7 for 100ms/cycle.

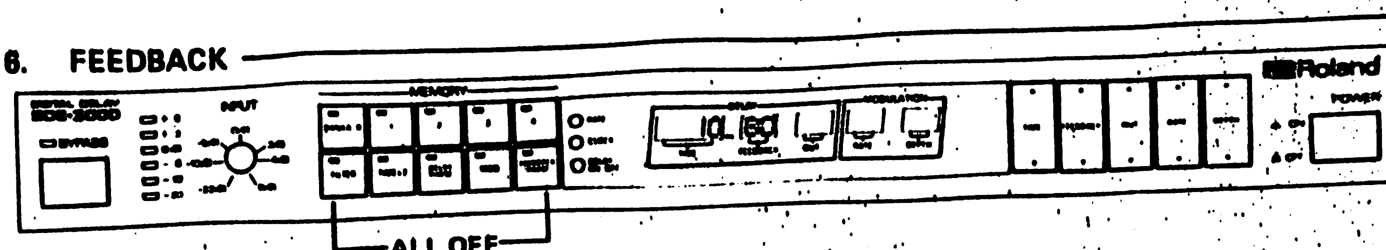


5. FREQUENCY RESPONSE



TEST POINT: DELAY OUT (connect to AC voltmeter)
5-1. Set UNIGAIN (Rear panel) to +4dBm and DELAY TIME to X1. Other functional switches OFF.
5-2. Connect AG to INPUT jack. Set AG for −10dBm, 1kHz, sine.
5-3. Adjust INPUT ATT for −10dBm reading.
5-4. Reset AG to 8.5kHz. Adjust VR4 for −10.2dBm rereading.
5-5. Press DELAY TIME X2 (ON). Reset AG for 400Hz, −10dBm.
5-6. Adjust INPUT ATT for −10dBm reading.
5-7. Reset AG to −10dBm, 5kHz. Adjust VR5 for −10.2dBm reading.

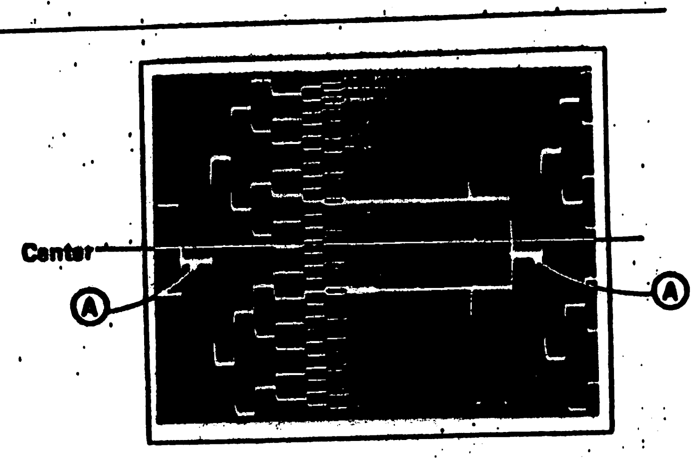
6. FEEDBACK

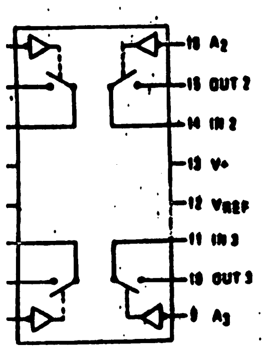
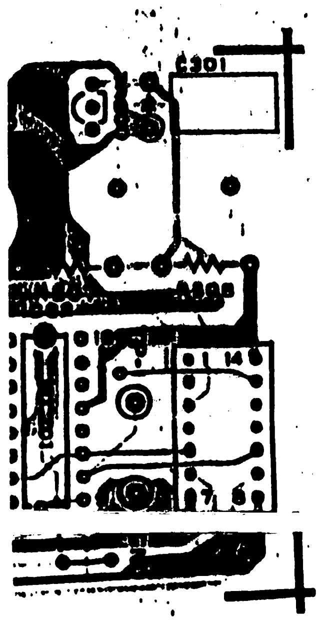
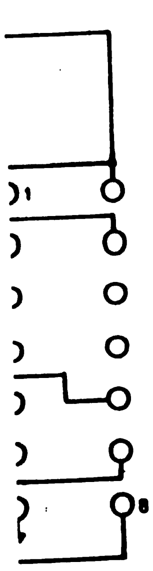


6-1. Set DELAY TIME to X1.
6-2. Turn VR3 fully clockwise. All INPUT level LEDs will light up from −20 to +6.
6-3. Gradually reverse VR3 until +6 and +3 LEDs go off completely.
6-4. Confirm the following:
With FEEDBACK set at 81, +3 and +6 light again.
With FEEDBACK 79, all level LEDs go off one by one.

7. D/A OFFSET

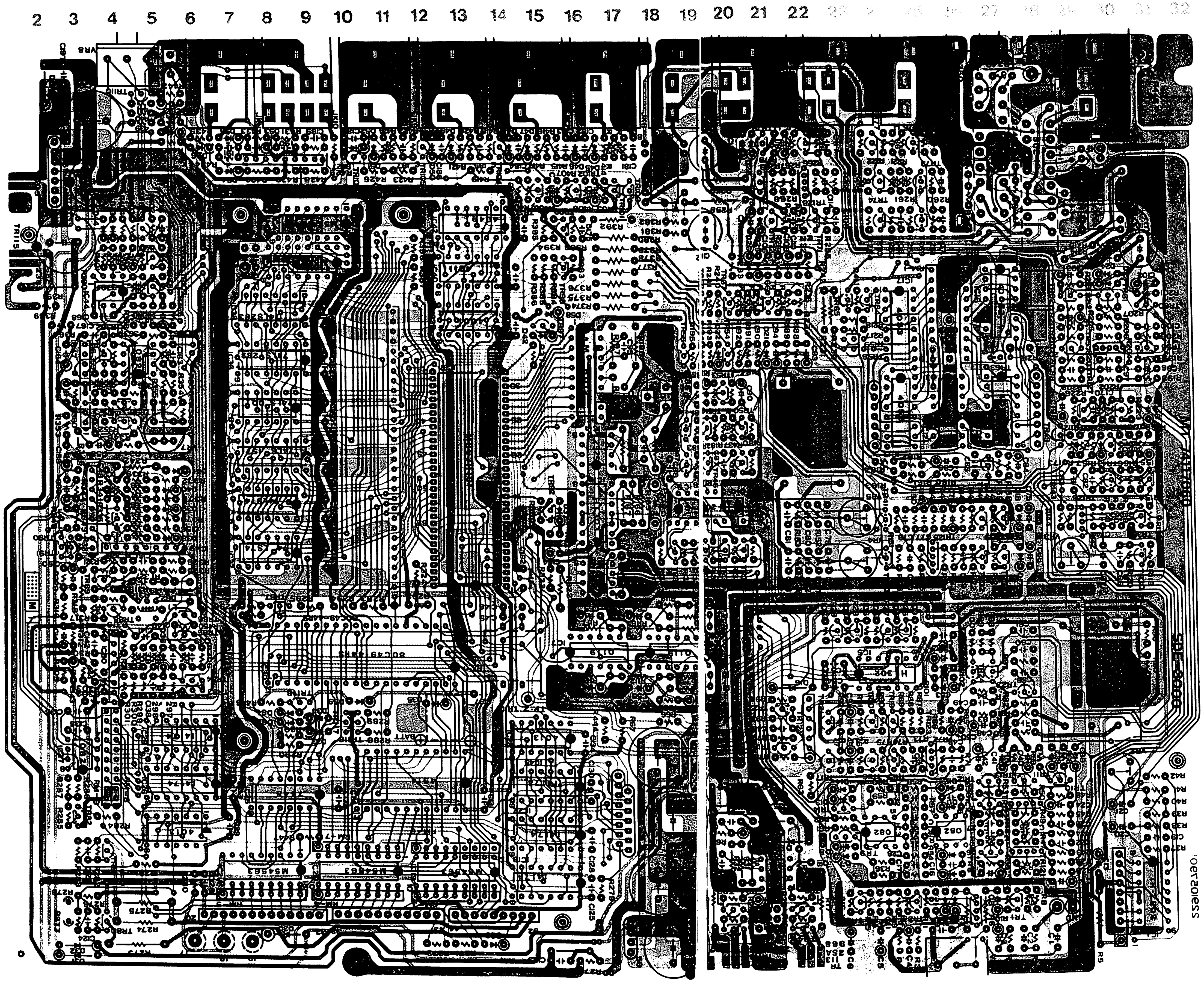
TEST POINT: TP-1 (connect to scope, Y-axis or V IN − DC couple)
Connect TP-2 to X-axis or EXT TRIG.
7-1. Set UNIGAIN to −20dBm and DELAY TIME to X1.
7-2. Connect AG to INPUT jack. Set AG for −16dBm, 100Hz, sine.
7-3. Adjust scope's VOLTS/DIV-VAR to show a pattern similar to that in the photo.
7-4. Adjust VR6 so that "A" is on the center graticule.



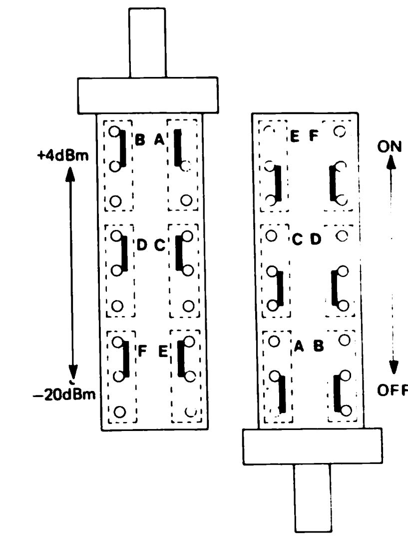




SDE-3000 MAIN BOARD

7411706026
(pcb 2291057901)



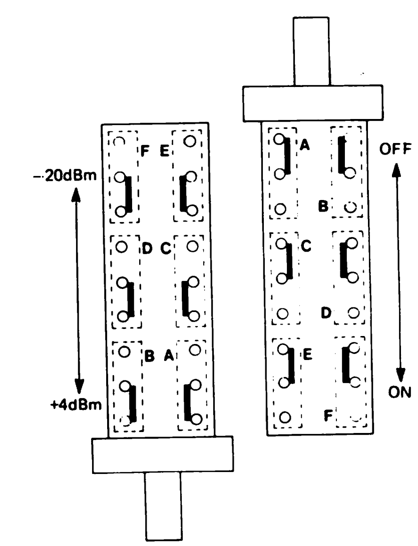
SW2
UNIGAIN(SUF-12)



SW1
BYPASS(SUE-12)

Top View

SW1
BYPASS(SUE-12)

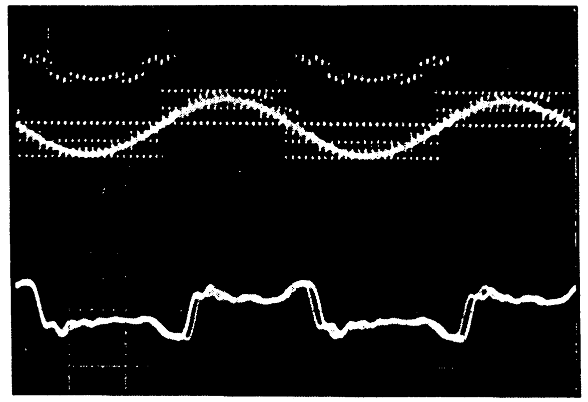


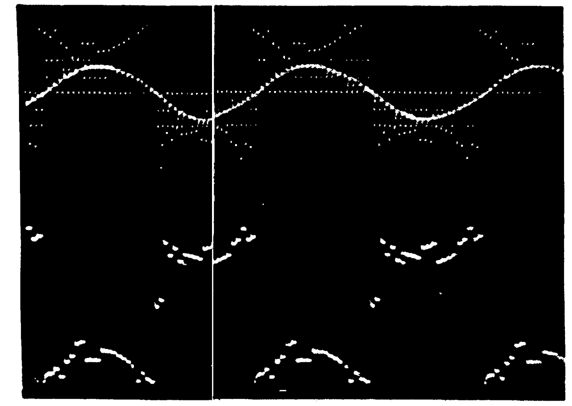
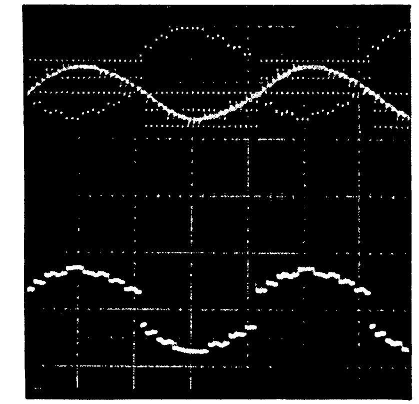
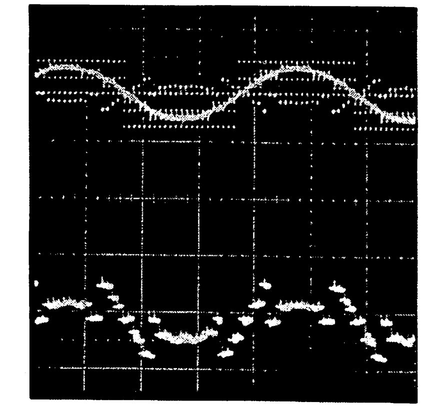
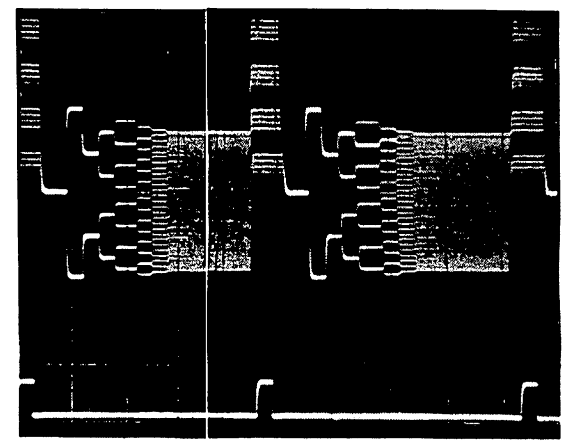
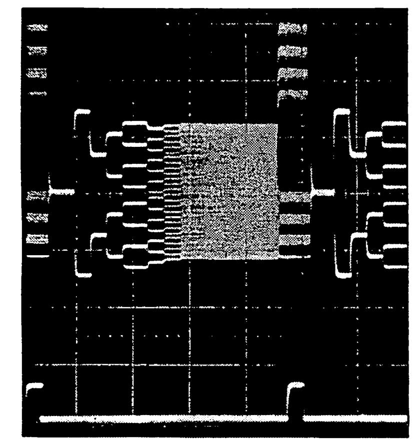
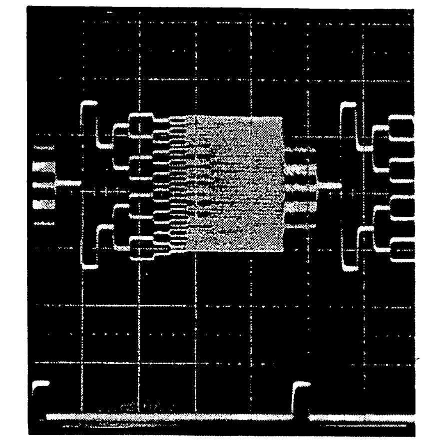
SW2
UNIGAIN(SUF-12)

Bottom View

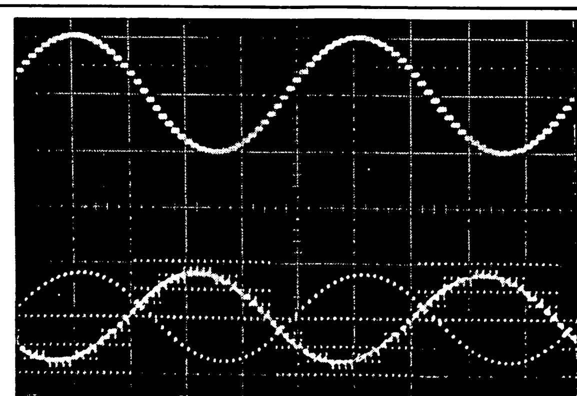
EXAMPLES OF RAM FAILURE
—No data on one RAM pin of Main Controller—

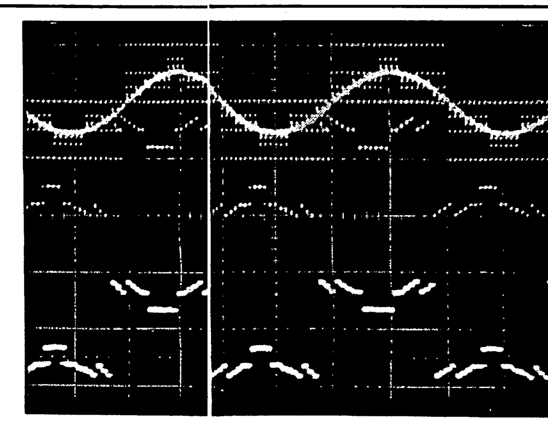
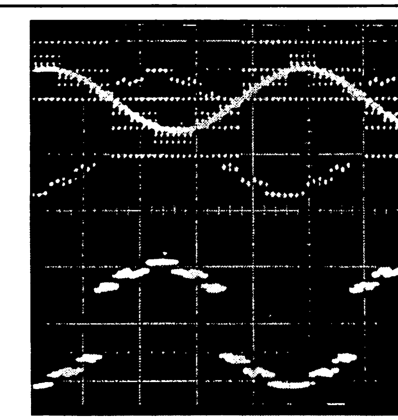
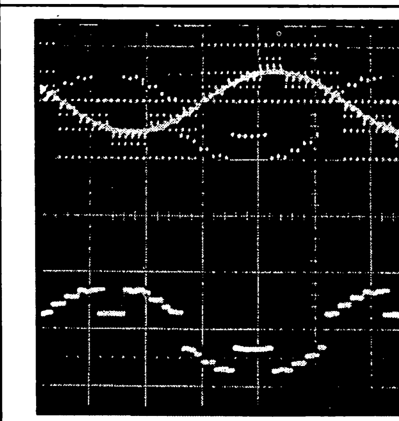
SDE-1000

INPUT −18dBm 1kHz	RAM1 (IC11)
RAM1 defective RAM1不良 IC28 pin6 5V/div TP-3 5V/div 0.2ms/div	

INPUT −18dBm 1kHz	RAM1 (IC11)	RAM2 (IC10)	RAM3 (IC9)
TP-3 5V/div IC16 pin6 2V/div 0.2ms/div			
TP-3 5V/div TP-1 20V/div 5μs/div			

SDE-3000

INPUT −10dBm 1kHz	
All RAMs intact 全RAM正常 TP-1 TR45/TR50 emitter	

INPUT −10dBm 1kHz	RAM1	RAM2	RAM3
TP-1 TR45/TR50 emitter 0.2ms/div			
TP-1 TP-2 5μs/div	